Product Specification

PE42672 DIE

SP7T UltraCMOS™ 2.75 V Switch 100 – 3000 MHz, +67 dBm IIP3

Figure 1. Functional Diagram

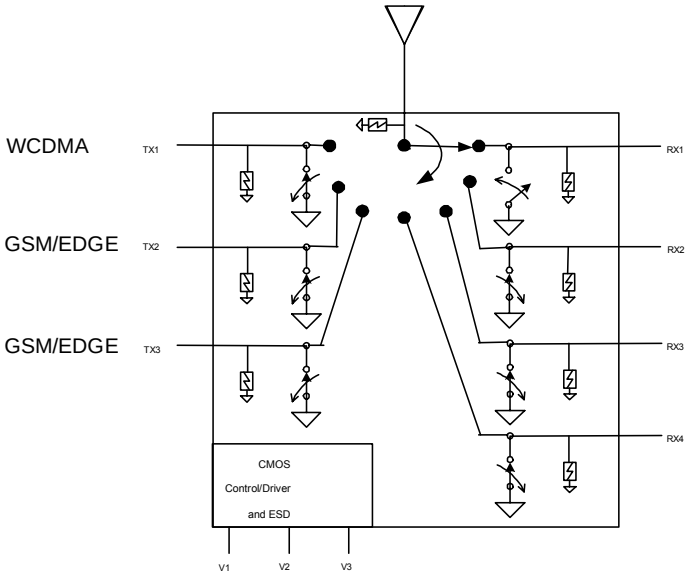
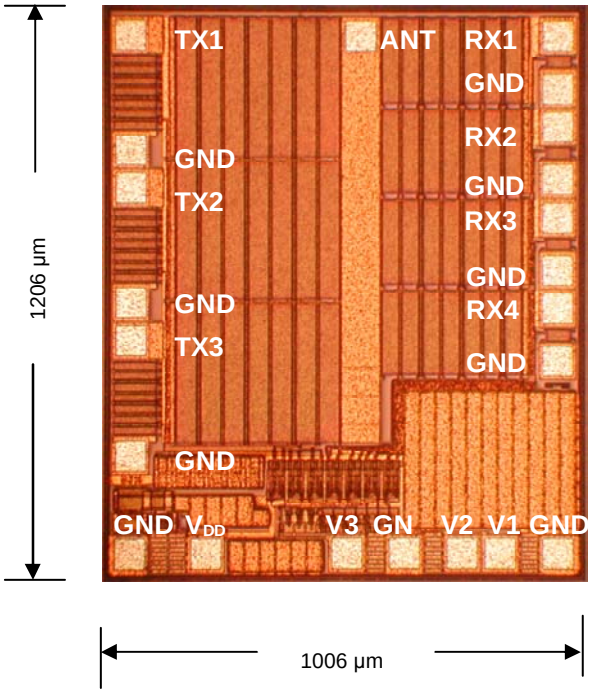


Figure 2. Die Top View*



* Dimensions shown are drawn die size.

Features

- Dedicated TX1 port for WCDMA, TX2 and TX3 ports for GSM/EDGE
- Three pin CMOS logic control with integral decoder/driver
- Exceptional harmonic performance: $2f_o$ = -85 dBc and $3f_o$ = -78.5 dBc
- Low TX insertion loss: 0.60 dB at 900 MHz, 0.70 dB at 1900 MHz
- TX – RX Isolation of 44 dB at 900 MHz, 38 dB at 1900 MHz
- 1000 V HBM ESD tolerance RF ports
- +67 dBm IIP3
- -109 dBm IMD3
- No blocking capacitors required

Product Description

The PE42672 is a HaRP™-enhanced SP7T RF Switch developed on the UltraCMOS™ process technology. It addresses the specific design needs of the Quad-Band GSM Handset Antenna Switch Module Market for use in GSM/EDGE/PCS/DCS/WCDMA handsets. The switch is comprised of three TX ports and four RX ports. TX1 is designed for WCDMA and TX2 and TX3 are designed for GSM/EDGE. The four symmetric RX ports can be used for GSM/EDGE/PCS RX. On-chip CMOS decoder logic facilitates three-pin low voltage CMOS control, while high ESD tolerance of 1000 V at RF ports, no blocking capacitor requirements, and on-chip SAW filter over-voltage protection devices make this the ultimate in integration and ruggedness.

Peregrine's HaRP™ technology enhancements deliver high linearity and exceptional harmonics performance. It is an innovative feature of the UltraCMOS™ process, providing performance superior to GaAs with the economy and integration of conventional CMOS.

Table 1. Target Electrical Specifications @ 25 °C, V_{DD} = 2.75 V

Parameter	Condition	Typ	Units
Insertion loss[1]	TX - Ant (850 / 900) TX - Ant (1800 / 1900) TX - Ant (2100 WCDMA) RX - Ant (850 / 900) RX - Ant (1800 / 1900)	0.6 0.7 0.75 0.9 0.9	dB dB dB dB dB
Return Loss	Port under test in on state	20	dB
Isolation	TX - RX (850 / 900) TX - RX (1800 / 1900) TX - TX (850 / 900) TX - TX (1800 / 1900) TX1 - RX (1900 / 2100)	44 38 29 23 39	dB dB dB dB dB
2nd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-85 -84	dBc dBc
3rd Harmonic	TX 850 / 900 MHz, +35 dBm output power, 50 Ω TX 1800 / 1900 MHz, +33 dBm output power, 50 Ω	-78.5 -78.5	dBc dBc
IMD3 distortion at 2.14 GHz	TX1 Measured at 2.14 GHz at Ant port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	-109	dBm
WCDMA 2100 IIP3	TX1 Measured at 2.14 GHz at Ant port, input +20 dBm CW signal at 1.95 GHz and -15 dBm CW signal at 1.76 GHz	+67	dBm
Switching time	(10-90%) (90-10%) RF	2	µs

Note: 1. Insertion loss specified with optimal impedance matching.

Table 2. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Units
Temperature range	T_{OP}	-40		+85	°C
V_{DD} Supply Voltage	V_{DD}	2.65	2.75	2.85	V
I_{DD} Power Supply Current (V_{DD} = 2.75 V)	I_{DD}		13	50	µA
TX input power[2] (VSWR ≤ 3:1) 824-915 MHz	P_{IN}			+35	dBm
TX input power[2] (VSWR ≤ 3:1) 1710-1910 MHz				+33	
RX input power[2] (VSWR =1:1)	P_{IN}			+20	dBm
Control Voltage High	V_{IH}	1.4			V
Control Voltage Low	V_{IL}			0.4	V

Note: 2. Assumes RF input period of 4620 µs and duty cycle of 50%.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
V_{DD}	Power supply voltage	-0.3	4.0	V
V_I	Voltage on any input	-0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	-65	+150	°C
P_{IN}(50 Ω)	TX input power (50 Ω)[3,4] 824-915 MHz		+38	dBm
	TX input power (50 Ω)[3,4] 1710-1910 MHz		+36	
	RX input power (50 Ω)[3,4]		+23	
P_{IN} (∞:1)	TX input power (VSWR = (∞:1)[3,4] 824-915 MHz		+35	dBm
	TX input power (VSWR = (∞:1)[3,4] 1710-1910 MHz		+33	
V_{ESD}[5]	ESD Voltage, Digital Pins		500	V
	ESD Voltage, RF Pins		1000	

Note: 3. Assumes RF input period of 4620 µs and duty cycle of 50%.
4. V_{DD} within operating range specified in Table 2.
5. ESD Voltage (HBM, ML_STD 883 Method 3015.7)

Part performance is not guaranteed under these conditions. Exposure to absolute maximum conditions for extended periods of time may adversely affect reliability. Stresses in excess of absolute maximum ratings may cause permanent damage.

Table 4. Pin Descriptions

Pin No.	Pin Name	Description
1	ANT	RF Common – Antenna
2	TX1[7]	RF I/O - TX1
3	GND[6]	Ground
4	TX2[7]	RF I/O – TX2
5	GND[6]	Ground
6	TX3	RF I/O – TX3
7	GND[6]	Ground
8	GND[6]	Ground
9	V_{DD}	Supply
10	V3	Switch control input, CMOS logic level
11	GND[6]	Ground
12	V2	Switch control input, CMOS logic level
13	V1	Switch control input, CMOS logic level
14	GND[6]	Ground
15	GND[6]	Ground
16	RX4[7]	RF I/O – RX4
17	GND[6]	Ground
18	RX3[7]	RF I/O – RX3
19	GND[6]	Ground
20	RX2[7]	RF I/O – RX2
21	GND[6]	Ground
22	RX1[7]	RF I/O – RX1

Notes: 6. Bond wires should be physically short and connected to ground plane for best performance.
7. Blocking capacitors needed only when non-zero DC voltage present.

Figure 3. Pad Configuration (Top View)

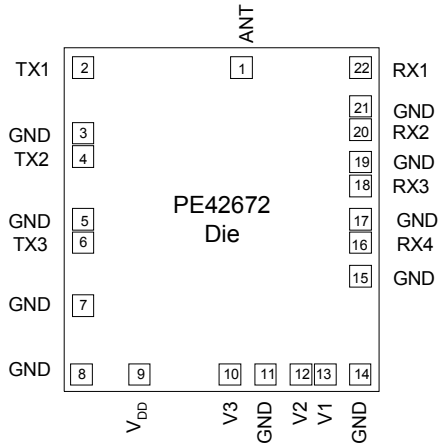


Table 5. Truth Table

Path	V3	V2	V1
RX1 - ANT	0	0	0
RX2 - ANT	0	0	1
RX3 - ANT	0	1	0
RX4 - ANT	0	1	1
TX1 - ANT	1	0	0
TX2 - ANT	1	0	1
TX3 - ANT	1	1	0
All Off	1	1	1

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Table 6. Ordering Information

Order Code	Description	Package	Shipping Method
42672-90	PE42672-DIE-D	Film Frame	Wafer (Gross Die / Wafer Quantity)
42672-99	PE42672-DIE-400G	Waffle Pack	400 Dice / Waffle Pack
42672-00	PE42672-DIE-1H	Evaluation Kit	1/ box

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Data Sheet Identification

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Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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