

TOSHIBA CMOS Linear Integrated Circuit Silicon Monolithic

TC75S101F, TC75S101FU, TC75S101FE

Single Operational Amplifier (Input and Output Full Range)

Features

- Input and Output Full Range
- Low-input offset voltage : $V_{IO} = 3.0 \text{ mV (max.)}$
- Low-input bias current : $I_I = 0.1 \text{ pA (typ.)}$
- Built-in phase-compensated op-amp, obviating the need for any external device
- Ultra-small package

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Supply voltage		V_{DD}, V_{SS}	6	V
Differential input voltage		DV_{IN}	± 6	V
Input voltage		V_{IN}	V_{DD} to V_{SS}	V
Power dissipation	TC75S101F/FU	P_D	200	mW
	TC75S101FE		100	
Operating temperature		T_{opr}	-40 to 85	°C
Storage temperature		T_{stg}	-55 to 125	°C

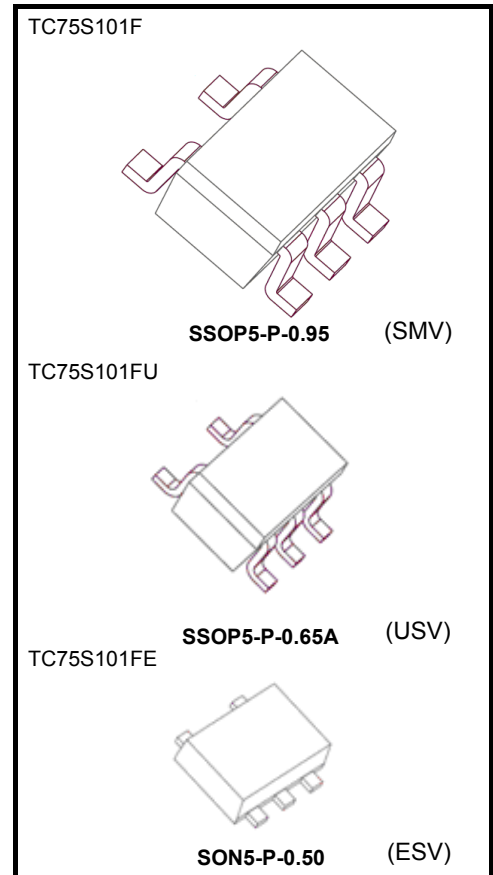
Product device does not use these for open-loop configuration.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc)

Operating Conditions

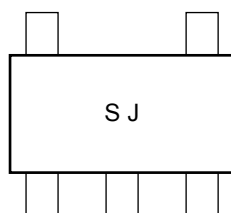
Characteristics	Symbol	Rating	Unit
Supply voltage	V_{DD}, V_{SS}	1.5 to 5.5	V
		± 0.75 to 2.75	



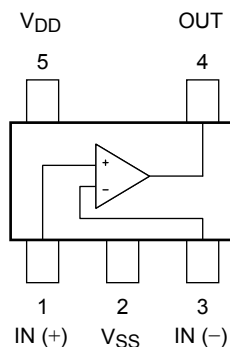
Weight

- SSOP5-P-0.95 : 14 mg (typ.)
- SSOP5-P-0.65A : 6.2 mg (typ.)
- SON5-P-0.50 : 3.0 mg (typ.)

Marking (top view)



Pin Connection (top view)



Electrical Characteristics

DC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	$R_S = 1\Omega$, $R_F = 100\text{ k}\Omega$	—	1.2	3.0	mV
Input offset current	I_{IO}	—	—	0.1	—	pA
Input bias current	I_I	—	—	0.1	—	pA
Common mode input voltage	CMV_{IN}	$R_S = 1\Omega$, $R_F = 100\text{ k}\Omega$	0	—	3.0	V
Voltage gain (open loop)	G_V	—	40	110	—	dB
Maximum output voltage	V_{OH}	$R_L \geq 100\text{ k}\Omega$	2.9	—	—	V
	V_{OL}	$R_L \geq 100\text{ k}\Omega$	—	—	0.1	
Common mode input signal rejection ratio	CMRR	$V_{IN} = 0.0\text{ to }3.0\text{ V}$	50	66	—	dB
Supply voltage rejection ratio	SVRR	$V_{DD} = 1.8\text{ to }6.0\text{ V}$	65	90	—	dB
Supply current	I_{DD}	—	—	63	90	μA
Source current	I_{source}	—	70	110	—	μA
Sink current	I_{sink}	—	800	1500	—	μA

DC Characteristics ($V_{DD} = 1.8\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input offset voltage	V_{IO}	$R_S = 1\Omega$, $R_F = 100\text{ k}\Omega$	—	0.9	3.0	mV
Input offset current	I_{IO}	—	—	0.1	—	pA
Input bias current	I_I	—	—	0.1	—	pA
Common mode input voltage	CMV_{IN}	$R_S = 1\Omega$, $R_F = 100\text{ k}\Omega$	0	—	1.8	V
Voltage gain (open loop)	G_V	—	40	100	—	dB
Maximum output voltage	V_{OH}	$R_L \geq 100\text{ k}\Omega$	1.7	—	—	V
	V_{OL}	$R_L \geq 100\text{ k}\Omega$	—	—	0.1	
Supply current	I_{DD}	—	—	57	80	μA
Source current	I_{source}	—	50	95	—	μA
Sink current	I_{sink}	—	700	1450	—	μA

AC Characteristics ($V_{DD} = 3.0\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	$A_V = 0\text{ dB}$	—	0.15	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	$A_V = 40\text{ dB}$	—	0.62	—	MHz

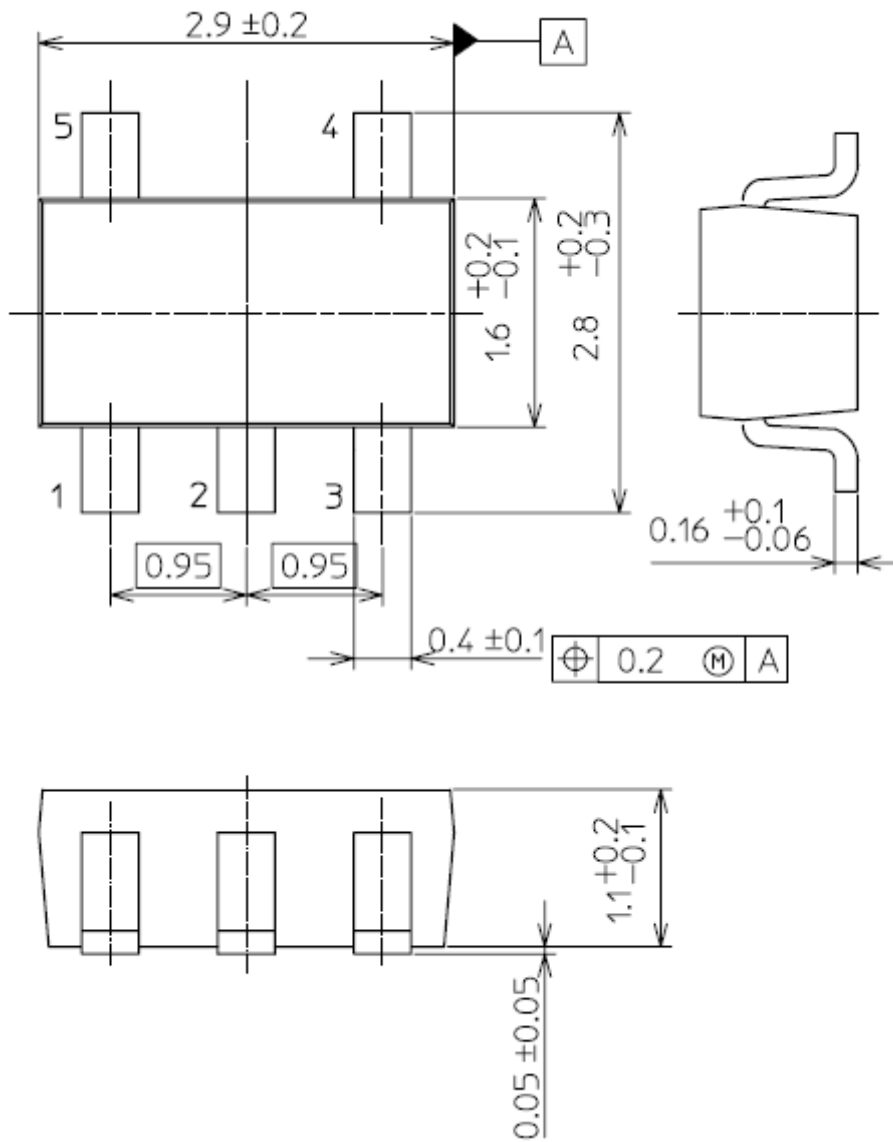
AC Characteristics ($V_{DD} = 1.8\text{ V}$, $V_{SS} = \text{GND}$, $T_a = 25^\circ\text{C}$)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Slew rate	SR	$A_V = 0\text{ dB}$	—	0.14	—	$\text{V}/\mu\text{s}$
Unity gain cross frequency	f_T	$A_V = 40\text{ dB}$	—	0.55	—	MHz

Package Dimensions

SMV

Unit: mm

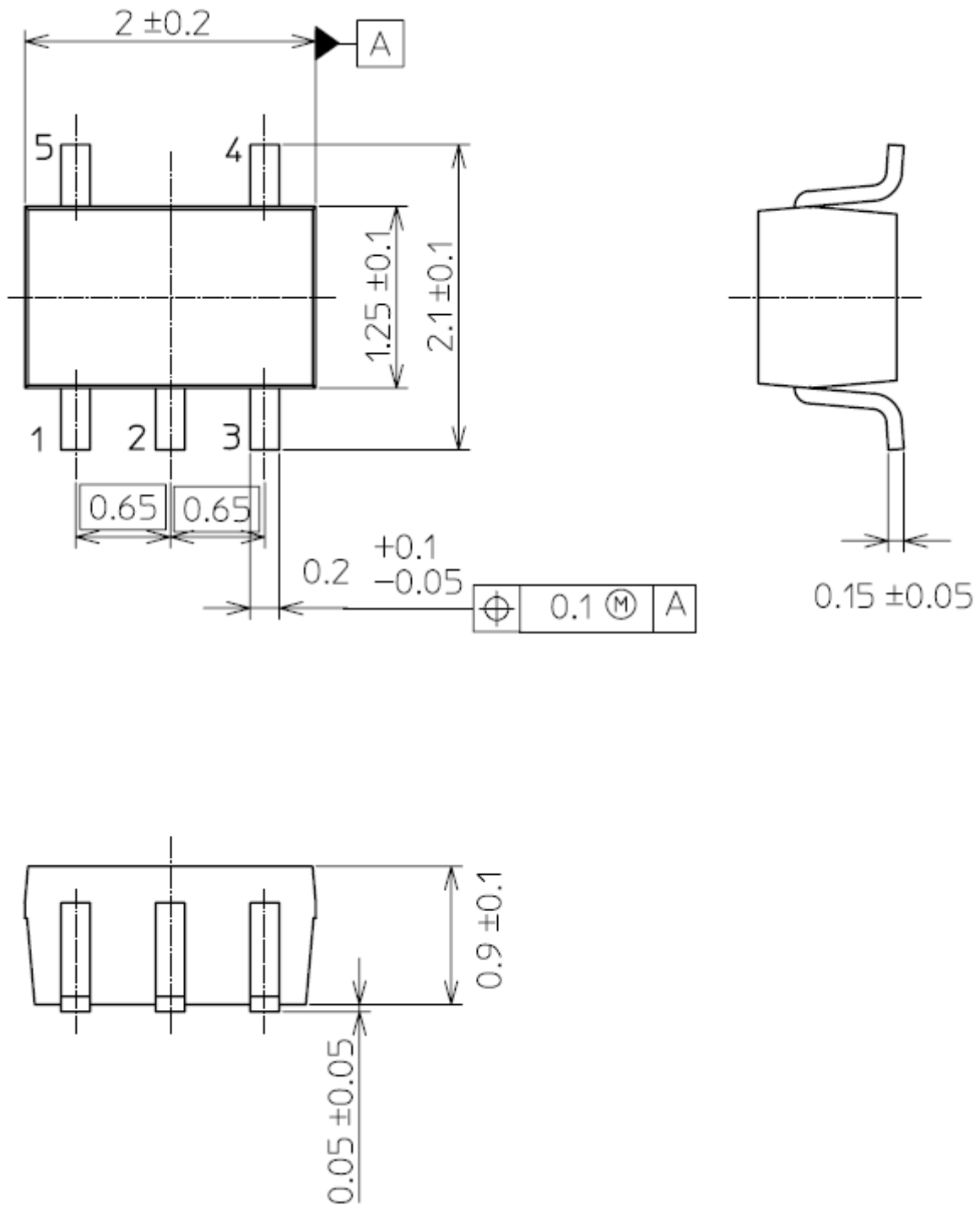


Weight: 14 mg (typ.)

Package Dimensions

USV

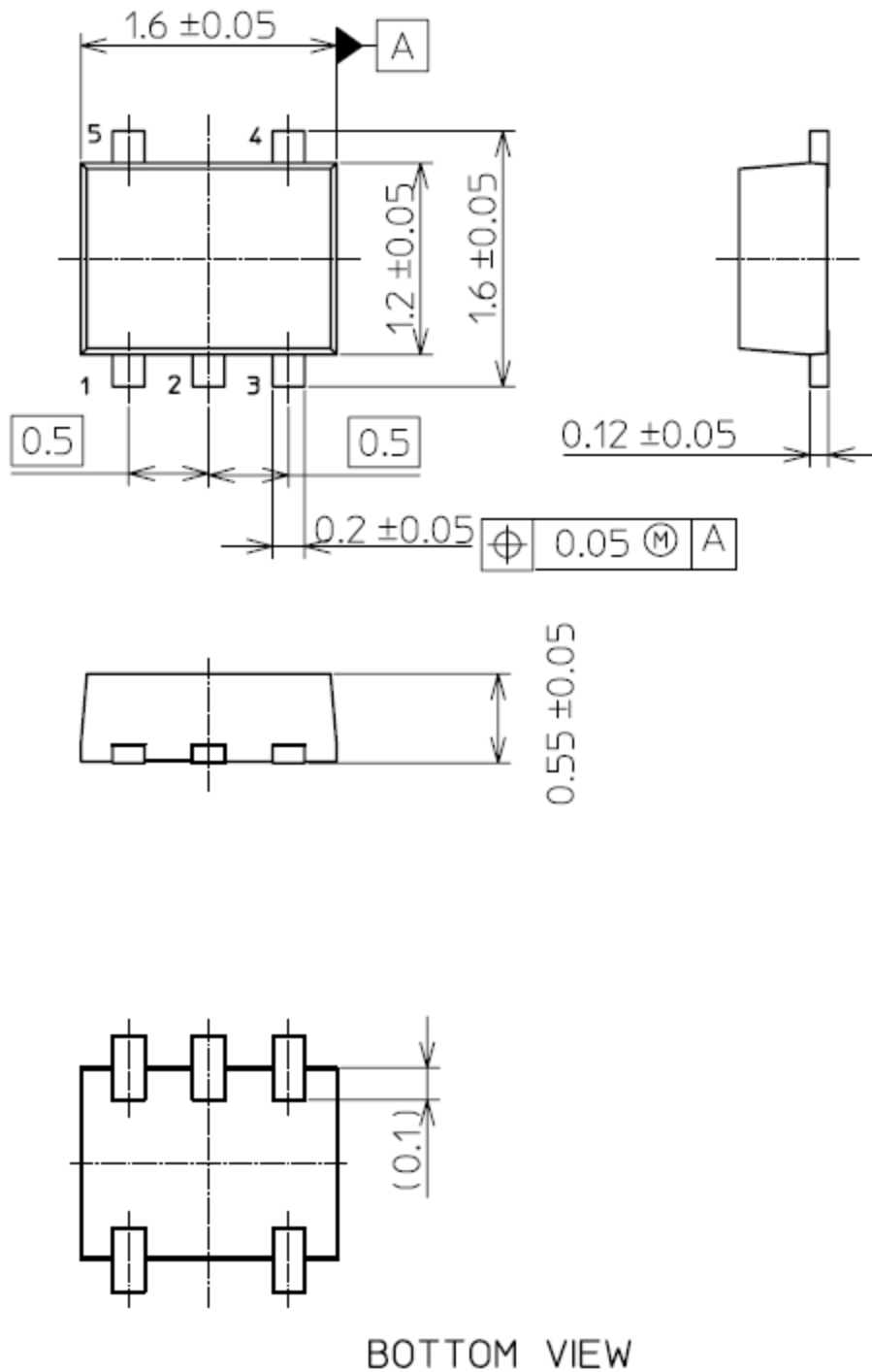
Unit: mm



Weight: 6.2 mg (typ.)

Package Dimensions
ESV

Unit: mm



Weight: 3.0 mg (typ.)

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