

2SK3862

Silicon N-channel junction FET

For impedance conversion in low frequency

For electret capacitor microphone

■ Features

- Low noise voltage NV
- High voltage gain GV
- Thin package: TSSSMini3-F1 (1.2 mm × 1.2 mm × 0.33 mm)

■ Package

- Code
TSSSMini3-F1
- Pin Name
1: Drain
2: Source
3: Gate

■ Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Drain-source voltage (Gate open)	V_{DSO}	20	V
Drain-gate voltage (Souece open)	V_{DGO}	20	V
Drain-source current (Gate open)	I_{DSO}	2	mA
Drain-gate current (Souece open)	I_{DGO}	2	mA
Power dissipation	P_D	100	mW
Operating ambient temperature	T_{opr}	-20 to +80	°C
Storage temperature	T_{stg}	-55 to +125	°C

■ Marking Symbol: 5D

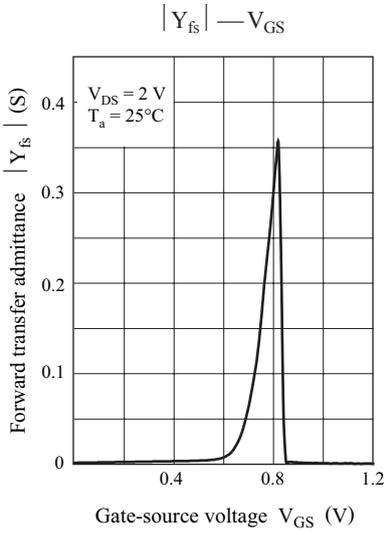
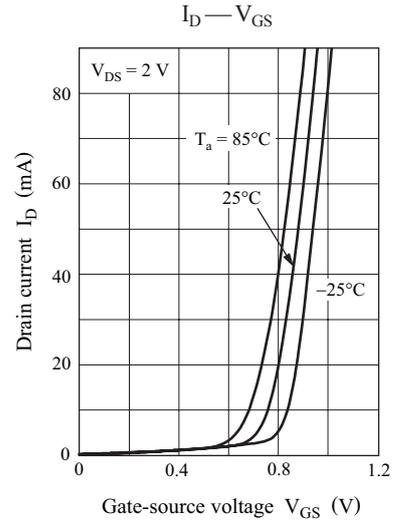
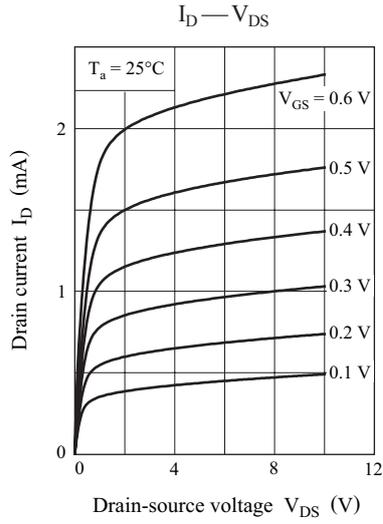
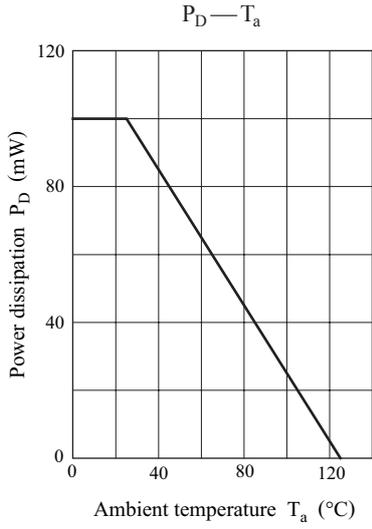
■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain current *1	I_D	$V_{DS} = 2.0\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$	100		470	μA
Drain-source current *2	I_{DSS}	$V_{DS} = 2.0\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%, V_{GS} = 0$	107		460	μA
Forward transfer conductance	$ Y_{fs} $	$V_D = 2.0\text{ V}, V_{GS} = 0, f = 1\text{ kHz}$	660	1500		μS
Noise voltage *3	NV	$V_D = 2.0\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}, A\text{-curve}$			4	μV
Voltage gain	G_{V1}	$V_D = 2.0\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}, e_G = 10\text{ mV}, f = 1\text{ kHz}$	-5.0	-1.0		dB
	G_{V2}	$V_D = 12\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}, e_G = 10\text{ mV}, f = 1\text{ kHz}$	-3.0	3.0		
	G_{V3}	$V_D = 1.5\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}, e_G = 10\text{ mV}, f = 1\text{ kHz}$	-7.0	-1.5		
Voltage gain difference	$\Delta G_V \cdot f $ *4	$V_D = 2.0\text{ V}, R_d = 2.2\text{ k}\Omega \pm 1\%$ $C_O = 5\text{ pF}, e_G = 10\text{ mV}$ $f = 1\text{ kHz to } 70\text{ Hz}$	0		1.7	
	$ G_{V1} - G_{V3} $			0.5	2.0	dB
Gate resistance	R_g		8	10		$\text{G}\Omega$

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.
 2. A protection diode is built-in between gate and source of transistor. However if forward current flows between gate and source transistor might be damaged. So please be careful not insert reverse.
 3. *1: I_D is assured for I_{DSS} .
 *2: Rank classification

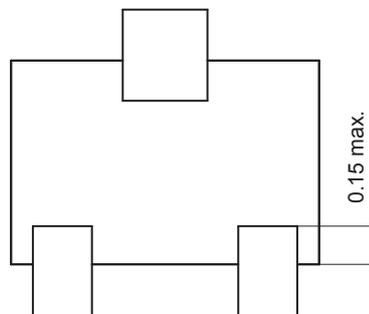
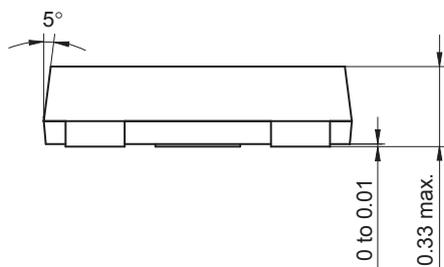
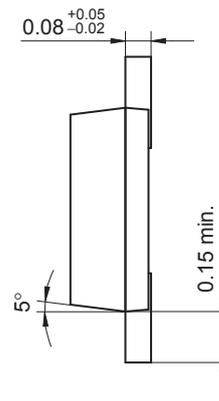
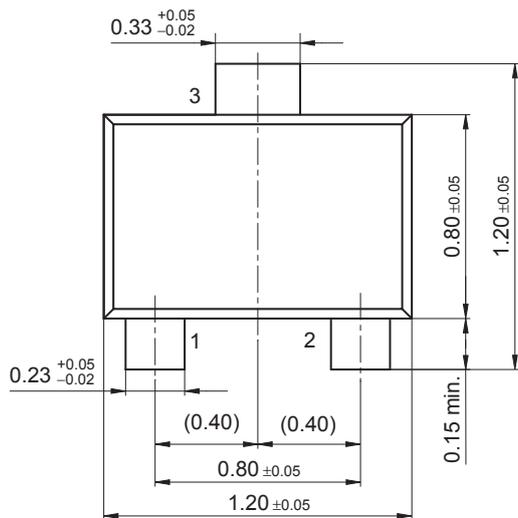
Rank	R	S	T	U
$I_{DSS} (\mu\text{A})$	107 to 150	130 to 220	180 to 315	285 to 460

*3: NV is assured for design.
 *4: $\Delta |G_V \cdot f|$ is assured for AQL 0.065. (The measurement method is used by source-grounded circuit.)



TSSSMini3-F1

Unit: mm



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