SONY

CXG1173UR

High Power SPDT Switch with Logic Control

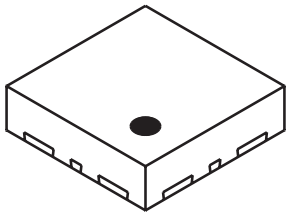
Description

The CXG1173UR can be used in wireless communication systems, for example, CDMA handsets, W-CDMA handsets, 2.4GHz WLAN.

The CXG1173UR has on-chip logic for operation with 1 CMOS control inputs.

The Sony J-FET process is used for low insertion loss and on-chip logic circuit.

12 pin UQFN (Plastic)



Features

- Low insertion loss: 0.3dB@900MHz, 0.45dB@1.95GHz
- 1 CMOS compatible control line
- Small package size: 12-pin UQFN

Applications

- Antenna switch for cellular handsets
  W-CDMA, CDMA
- Antenna switch for cellular handsets
  2.4GHz WLAN IEEE 802.11b, 802.11g

Structure

GaAs J-FET MMIC

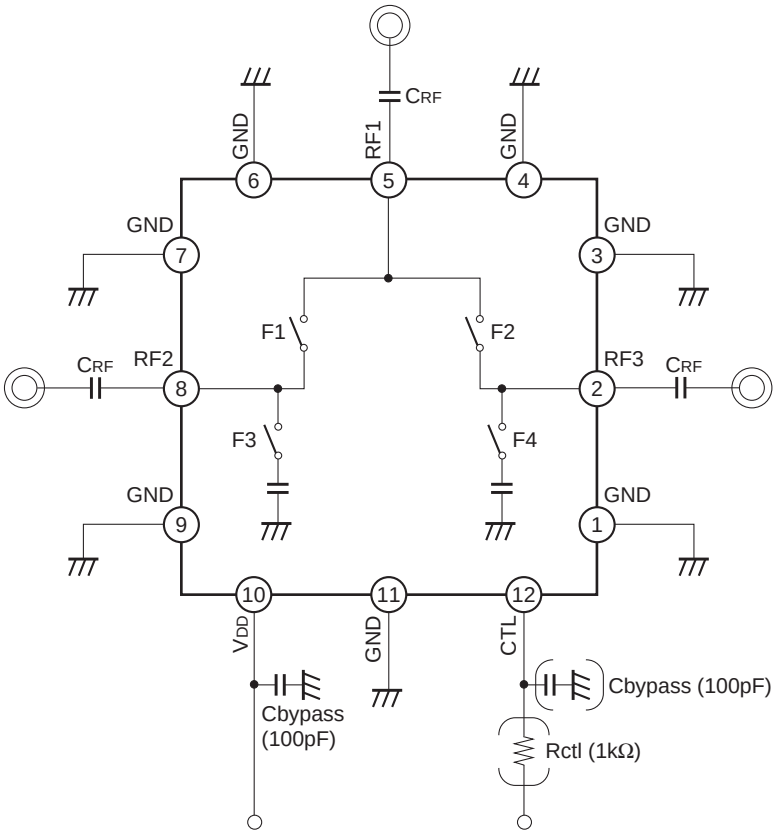
Absolute Maximum Ratings (Ta = 25°C)

• Bias voltage	V_{DD}	7	V
• Control voltage	Vctl	5	V
• Operation temperature	Topr	–35 to +85	°C
• Storage temperature	Tstg	–65 to +150	°C

GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

E03Y12-PS

Block Diagram and Recommended Circuit



When using this IC, the following external components should be used:

Rctl: This resistor is used to improve ESD performance. 1kΩ is recommended.

C_{RF}: This capacitor is used for RF De-coupling and must be used all application.

Cbypass: This capacitor is used for DC line filtering. 100pF is recommended.

Truth Table

CTL	ON State	F1	F2	F3	F4
H	RF1 – RF2	ON	OFF	OFF	ON
L	RF1 – RF3	OFF	ON	ON	OFF

DC Bias Condition (Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	2.0	3.0	3.6	V
Vctl (L)	0	—	0.4	V
V_{DD}	2.5	3.0	3.6	V

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	900MHz		0.30	0.50	dB
		1950MHz		0.45	0.65	dB
Isolation	ISO.	900MHz	24	30		dB
		1950MHz	18	25		dB
VSWR	VSWR	50Ω		1.2	1.5	—
Switching speed	TSW			2	5	µs
1dB compression input power	P1dB	*1, *2	34			dBm
Input IP3	IIP3	*3	55	63		dBm
ACLR	ACLR1	±5MHz, *1		–60	–50	dBc
	ACLR2	±10MHz, *1		–65	–55	dBc
	ACLR3	±900kHz, *2		–60	–50	dBc
	ACLR4	±1.98MHz, *2		–65	–55	dBc
Harmonics	2fo	*1		–75	–55	dBc
	3fo	*1		–75	–60	dBc
	2fo	*2		–75	–55	dBc
	3fo	*2		–75	–60	dBc
Bias current	I_{DD}	V_{DD} = 3.0V		65	100	µA
Control current	Ictl	Vctl (H) = 3.0V		15	30	µA

*1 Pin = 25dBm, 0/3.0V control, V_{DD} = 3.0V, 1920 to 1980MHz

*2 Pin = 25dBm, 0/3.0V control, V_{DD} = 3.0V, 900MHz

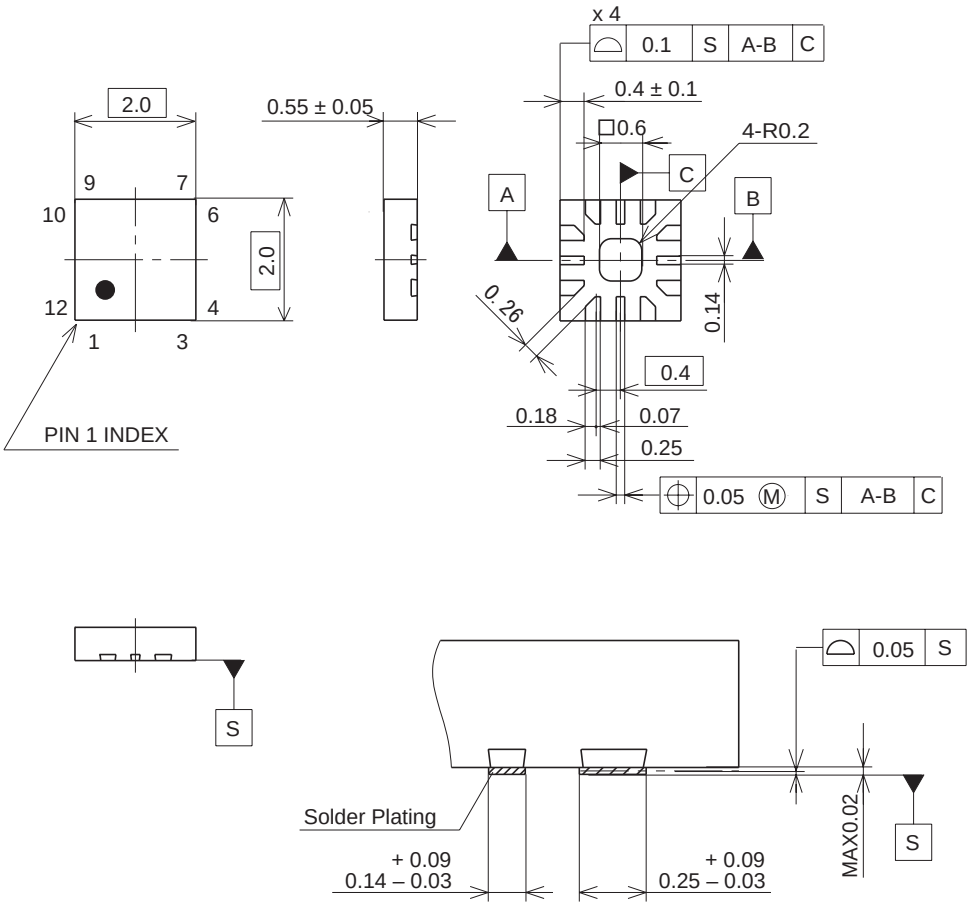
*3 Pin = 25dBm (900MHz) + 25dBm (901MHz), 0/3.0V control, V_{DD} = 3.0V

Pin Description

Pin No.	Symbol	Description
2	RF3	RF input/output. Connect capacitor (recommended value: 100pF) in use
5	RF1	RF input/output. Connect capacitor (recommended value: 100pF) in use
8	RF2	RF input/output. Connect capacitor (recommended value: 100pF) in use
10	V_{DD}	DC power supply
12	CTL	Logic control
1, 3, 4, 6, 7, 9, 11	GND	GND

Package Outline Unit: mm

12PIN UQFN（PLASTIC）



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	UQFN-12P-01
EIAJ CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm