1. Description

AP1458EQ is designed to charge high voltage photoflash capacitors quickly and efficiently and separated voltage supply for the controller stage and battery stage.
AP1458EQ monitors the transformer flyback voltage and controls the output photoflash capacitor voltage. The capacitor is held at a fully charged state without excessive power consumption. Automatic refresh function allows the capacitor to remain charged.
Enable pin initiates charging, Status pin indicates that the capacitor is fully charged.
The wide input voltage range from 1.8V to 5.5V, especially for 2 Cell NiCd/NiMH or 1-cell Li+, is suitable for using in different applications.
Only a few external components guarantee to use this chip very easy AP1458EQ comprises an IGBT driver for igniting flash tube.

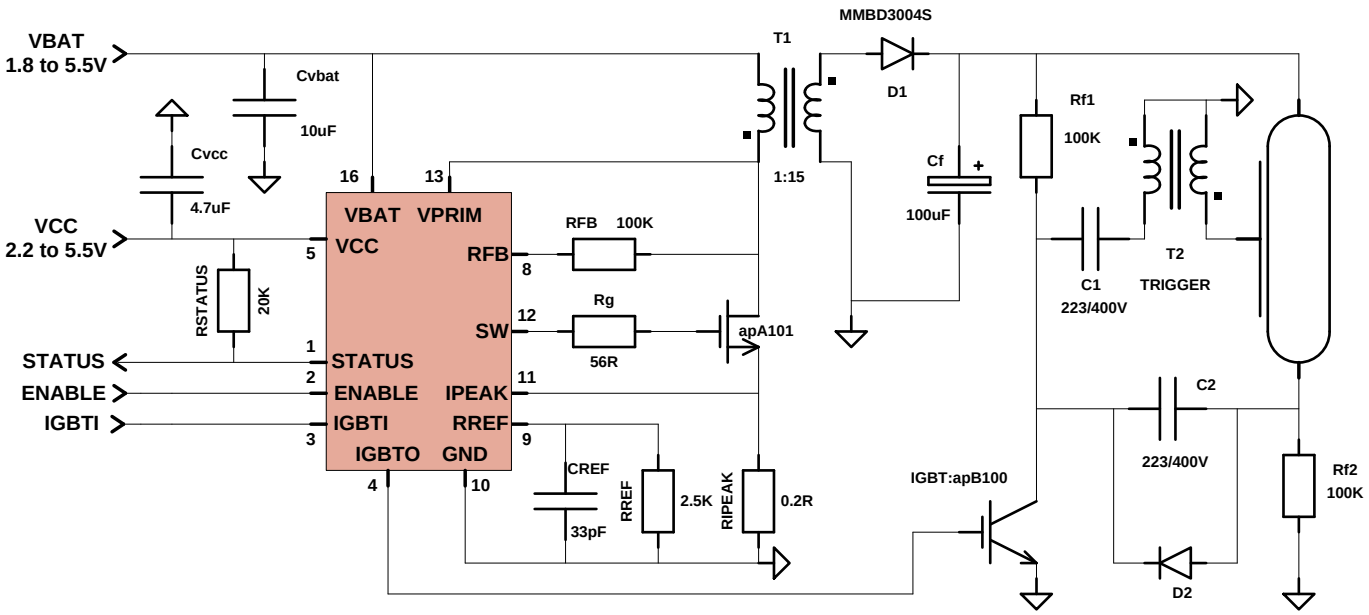
2. Features

- Wide input battery voltage range of 1.8V to 5.5V
- Fast Photoflash Charge Time
- Charges any size Photoflash capacitor
- Adjustable Output
- Controlled Peak Switch Current
- Automatic Refresh
- Output voltage detect from primary side
- Charge Complete Indicator
- Built-in IGBT driver for IGBT application
- Under voltage lock out (UVLO) detected at VBAT
- Package : TQFN16

3. Applications

- Digital Camera Flash Unit
- Film Camera Flash Unit
- High Voltage Power Supplies

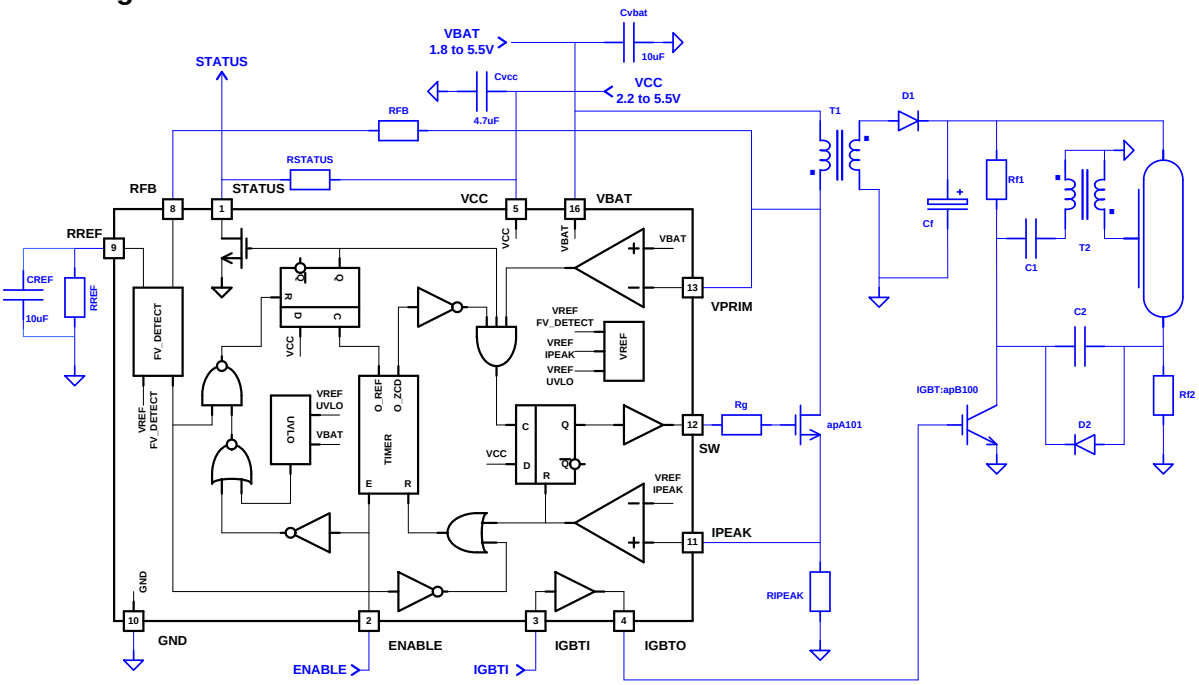
4. Typical Application



5. Pin/Pad Functions

Pin No.	Pad Name	I/O	Description
16	VBAT	IN	Battery Voltage Input. Must be locally bypassed with 10μF or larger ceramic capacitor. Apply 1.8V to 5.5V supply voltage to this pin.
1	STATUS	OUT	Open Drain status pin.. External resistor from this pin to VCC is needed. Status pin goes high when power delivery stops. Maximum drive capability for this pin is 2mA.
2	ENABLE	IN	Charging enable signal. Logic High level (>1.1V) enables AP1458EQ charging function. Logic Low level (0.3V or less) - AP1458EQ goes in disabled mode. If applied voltage level for ENABLE is bigger than VCC an extra resistor to this pin has to be added to reduce input current to 30uA.
3	IGBTI	IN	Input control signal for IGBT output buffer. Low input level = GND High input level = VCC If this pin is not used it has to be pulled up to VCC or pulled down to GND.
4	IGBTO	OUT	Powerful output, driving the needed pulse for an external IGBT.
5	VCC		Input Supply Pin. All internal analog and digital parts are supplied by this pin. Must be locally bypassed with 4.7μF or larger ceramic capacitor.
9	RREF	IN	Reference Resistor Pin for flash voltage detect. Place resistor RREF from this pin to GND. Needed value – 2-3 kΩ
8	RFB	IN	Flyback sense resistor pin for flash voltage detect. Place a resistor RFB from this pin to pin VPRIM. Value must be calculated for specified transformer turns ratio N: $RFB = RREF * \frac{DesiredOutputVoltage}{0.5 * TranformerT.Ratio}$
10	GND		Ground pin.
11	IPEAK	IN	Primary current sensing pin. Place a resistor RIPEAK from this pin to GND to adjust specified Ipeak current detection level: $RIPEAK = \frac{VrefIPEAK}{DesiredPeakCurrent}$
12	SW	OUT	Powerful output, driving an external MOS switch transistor.
13	VPRIM	IN	Transformer primary pin. Primary voltage is sensed to decide the turn on timing (ZCD).

6. Block Diagram



AP1458EQ comprises several main blocks :

- Flash Voltage Detect (FV_DETECT)
- IPEAK comparator (IPEAK)
- Zero Cross Detection comparator (ZCD)
- Timer
- Turn on Duty control and Status Latch
- Under Voltage Lock Out (UVLO)
- VREF

Short functional description for each of them is given below.

- Flash Voltage Detect

Detects transformer primary voltage set by external resistors RFB and RREF to sense whether the secondary flyback voltage corresponds to required maximum output voltage on the flash capacitor Cflash. When the target output voltage is reached the charging mode is terminated.

The resistor RREF must be on the range 2÷3kΩ, RREF is:

$$RFB = RREF * \frac{DesiredOutputVoltage}{0.5 * TranformerT.Ratio}$$

- IPEAK comparator (IPEAK)

Detects primary peak current adjusted by the resistor RIPEAK. When the voltage across RIPEAK exceeds VrefIPEAK the comparator output goes high resetting the latch and turning off M_switch. RIPEAK is calculated:

$$RIPEAK = \frac{VrefIPEAK}{DesiredPeakCurrent}$$

- Zero Cross Detection comparator (ZCD)

Detects zero current on secondary by primary side voltage value. After power MOS is switching off, the VPRIM voltage increases to VBAT+Vout/N. When the stored energy is completely transferred to the Flash voltage capacitor, secondary side current stops, and the transferred to the primary voltage is zero. The output of ZCD comparator goes high, setting the latch and turning on MOS switch.

- Timer

Generate REFRESH time and ZCD masking time.

- Under Voltage Lock Out (UVLO)

Protects the chip at low supply battery voltage.

- VREF

VREF block generates supply independent reference voltage to produce reference voltages for different blocks.

- Turn on Duty control and Status Latch

Turn on duty control latch manages MOS switch state. It is resetting from Ipeak comparator and sets from ZCD.

Status latch controls the modes of operation CHARGE/REFRESH. It is resetting from Flash voltage detect circuit and sets from ZCD timer output.

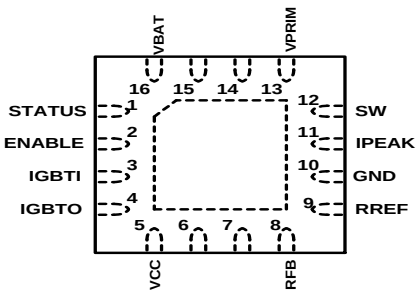
7. Absolute Maximum Ratings

Parameter	Symbol	Conditions
Power supply voltage	VCC	-0.3V to 7V
Battery supply voltage	VBAT	0 to 7V
All inputs and output voltages	V_{IO}	-0.3V to 7V
Operating Ambient Temperature Range	Ta	-40 to 85°C
Storage temperature range	T_{STORE}	-60 to 125°C

Exposure beyond specified conditions may affect device reliability or cause malfunction.

8. Package Information

TQFN16 PACKAGE



9. Electrical Characteristics

VCC = 2.2 ÷ 5.5V, VBAT=1.8÷5.5V, T_A = -40°C ÷ +85 °C

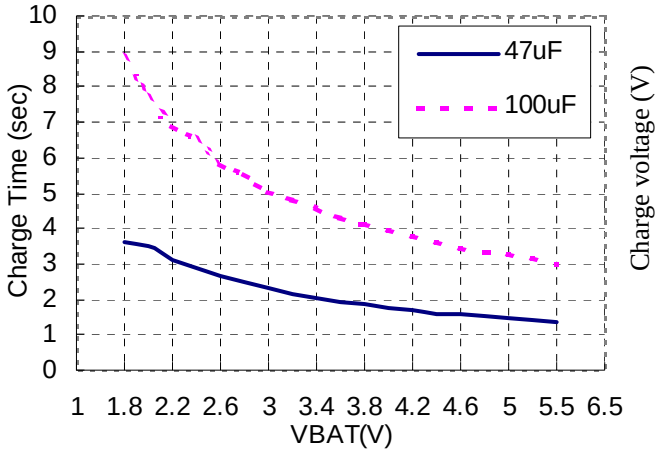
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Section : General						
Operating Supply voltage	VCC		2.2		5.5	V
Battery Supply voltage	VBAT		1.8		5.5	V
VPRIM Voltage	VPRIM	Turn ratio N=10 ÷25	13.8		35.5	V
Refresh charge time	Trefresh		1.2	2.2	2.5	msec
VBAT UVLO Threshold			1.49	1.5	1.62	V
Flash Voltage detect accuracy	U_O	U_O = 300V	U_O - 3%	U_O	U_O + 3%	V
Quiescent current	IQC	Not switching			0.5	mA
Quiescent current in disable	IQCo	VENABLE =0			5	μA
Average battery current		Charge mode(Ipeak adjust)	0.2		0.5	A
Reference voltage for IPEAK	VrefIPEAK			215	230	mV

Section : Enable Input Driver						
ENABLE Input current	I_I				5	μA
ENABLE High level input (Note 1)	V_{IH}		1.1			V
ENABLE Low level input	V_{IL}		-0.3		0.3	V
Section : Status						
STATUS Output High Level	V_{OH}	Ext R =20k to VCC			VCC	V
STATUS Output Low Level	V_{OL}	Ext R =20k to VCC			0.4	V
Section : IGBT Driver						
IGBT Driver Output Current	IOaver		30			mA
IGBT Driver Output Current	IOpeak		250			mA
IGBT Driver rise time	tr	Cload=10nF			250	ns
IGBT Driver fall time	tf	Cload=10nF			250	ns
Section : SW Driver						
SW Driver Ron (P and N)	Ron	At +/- 15 mA			30	Ohm
Peak SW Current	Aon	Average +/- 50 mA. (3.3V)	80			mA

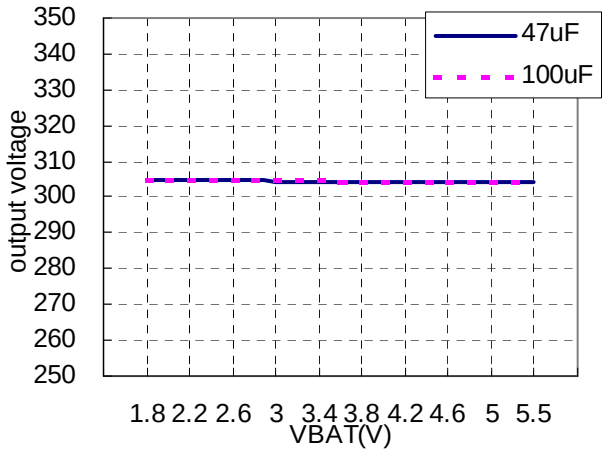
NOTE1: If applied voltage level for ENABLE is bigger than VCC an extra resistor to this pin has to be added to reduce input current to 30uA.

10. Typical Performance Characteristics

AP1458EQ Charge time (Vcc=3.0V)



AP1458EQ Output charge voltage

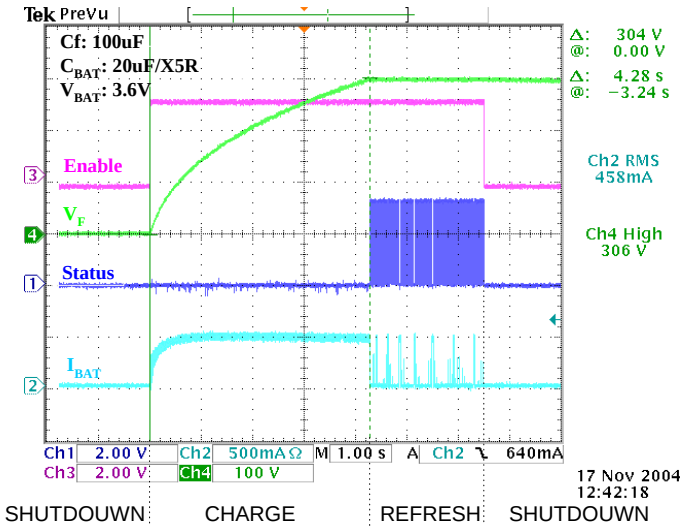


11. Operation

Overview

The following text focuses on the operation of the AP1458EQ.

The AP1458EQ uses an adaptive on-time/off-time control scheme to provide excellent efficiency and precise control of switching currents. Please refer to Block diagram for the following overview of the part's operation. At any given instant, the status latch determines which mode the AP1458EQ is in: "charging" or "refresh". In charging mode, the all analog blocks are enabled, providing power to charge photoflash capacitor Cf. The output voltage is monitored via the flyback pulse on the primary of the transformer. When the target output voltage is reached, the charging mode is terminated and the part enters the refresh mode. In refresh mode, the analog blocks are disabled, reducing quiescent current, while the timer is enabled. The timer simply generates a delay, after which the part reenters the charging mode. Once in the charging mode, the AP1458EQ will again provide power to the output until the target voltage is reached. The figure below is an oscillograph photo showing both the initial charging of the photoflash capacitor and the subsequent refresh action. The green waveform is the output voltage. The violet waveform is enable signal. The blue waveform shows the status pin. The mode of the part is indicated below the photo:



Power Delivery Block

The power delivery block consists of IPEAK comparator, ZCD comparator, FV_DETECT circuit, and SW latch. This circuit block contains all elements needed for charging and output voltage detection. To better understand the circuit operation, follow the subsequent description of one cycle of operation and refer to BLOCK DIAGRAM. Assume that initially there is no current in the primary or secondary of the transformer, so the output of ZCD comparator is high, while that of IPEAK comparator is low. The latch is thus set and the external power MOS switch, is turned on. Current increases linearly in the primary of the transformer at a rate determined by the VBAT voltage and the primary inductance of the transformer. As the current builds up, the voltage across the external IPEAK increases. When this voltage exceeds the VrefIPEAK, the output of IPEAK comparator goes high, resetting the latch and turning off external MOS. When MOS switch turns off, the secondary side current quickly jumps from zero current to the primary side current divided by N (the turns ratio of transformer T1). Diode D1 now conducts, providing power to the output. Since a positive voltage exists across the secondary winding of the transformer, the secondary current decreases linearly at a rate determined by the secondary inductance and the output voltage (neglecting the diode voltage drop). At this moment feeded back to primary voltage is secondary voltage divided by N. When the stored energy is completely transferred to the Flash voltage capacitor, secondary side current stops, and the transferred to the primary voltage is zero. The output of ZCD comparator goes high, setting the latch and turning on MOS switch. If the flayback pulse is too small to be sensed from ZCD (this situation is possible only at the charge beginning), the new charge pulse begins after fixed ZCD masking time (0.6ms to 1.2ms after switching off the external MOS). The power MOS switch will now remain on until the primary current again form VrefIPEAK voltage drop on IPEAK resistor. This cycle of operation repeats itself, automatically adjusting the On and Off times for the MOS.

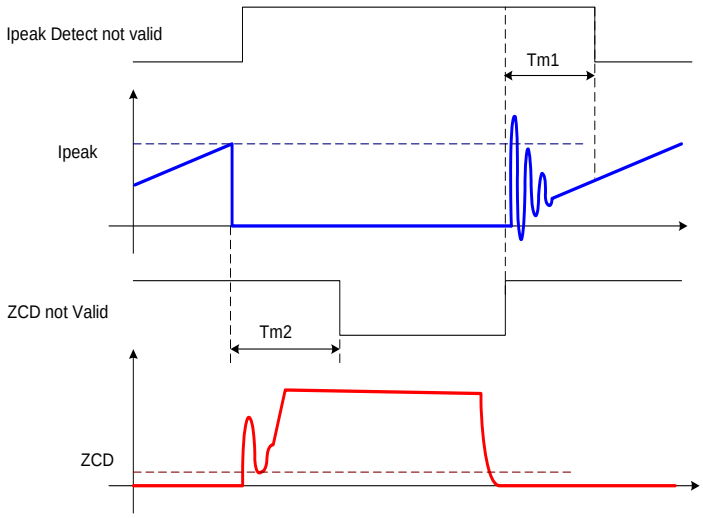
The previously described charging cycle must be halted when the output voltage reaches the desired value. The AP1458EQ monitors the output voltage via the flyback pulse in primary side. When MOS switch turns off, the secondary side conducts current turning on diode D1. Since the diode is conducting, the voltage across the secondary is nearly equal to VOUT . The voltage across the primary is therefore close to VOUT /N. A current proportional to VOUT /N flows through RFB resistor and into the RFB pin. The current flows out of the RREF pin through a resistor RREF creating a ground referred voltage. When this voltage exceeds an internal 0.5V reference voltage, the output of FV_DETECT circuit goes high which

resets the STATUS latch and timer. The Q output of the STATUS latch goes low, disabling the entire power delivery block.

After fixed REFRESH TIME (1.2ms to 2.4ms), the timer sends a set pulse to the STATUS latch, which puts the AP1458EQ into the charging mode.

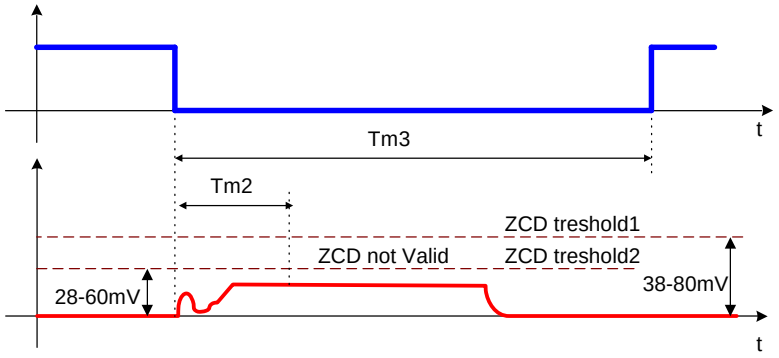
Leakage Spike Blanking

- Another function of the AP1458EQ is leakage spike blanking when the power MOS switch turns off. Right after external MOS turns off, the RREF is shorted for fixed time Tm2 (87ns to 226ns). Then comparator in FV_DETECT is disabled. This function may prevent the comparator from false tripping on the leakage inductance spike on the secondary transformer side. The same fixed delay time Tm2 is used for ZCD comparator protection.
- The time Tm1 (170ns to 250ns) is included to prevent the IPEAK comparator from the false leakage inductance spike right after switching On the external MOS.



Timer

- When the charging mode is terminated by flash voltage detect block a counter is enabled to give single pulse after refresh time (1.2ms to 2.5ms) to restart charging mode.
- The same counter is used to prevent false turn on of M_switch before correct ZCD function is possible (at low output voltage) generating M_switch off time Tm3 (0.6ms to 1.2ms) independent on ZCD function when charging starts:



UVLO

A protection system shutting down the CHIP when VBAT drops below 1.5V.

12. Applications Information

COMPONENT SELECTION

Choosing the Right Transformer
The flyback transformer plays a key role in any AP1458EQ application. A poorly designed transformer can result in inefficient operation. The following is a brief discussion of the issues relating to transformer design.

Transformer Turns Ratio
The turns ratio for the transformer, N, should be high enough so that the absolute maximum voltage ratings for the MOS power switch and VPRIM pin are not exceeded. When the power switch turns off, the voltage on the drain of the switch and VPRIM pin will "fly" up to the output voltage divided by N plus the battery voltage (neglecting the voltage drop across the rectifying diodes). **This voltage should not exceed the 38V (for VPRIM) and breakdown rating of the power MOS switch.** Choose the minimum N by the following formula.

$$N\min = \frac{DesiredOutputVoltage}{MIN(38V, MAX(Vds_{MOS})) - VBAT}$$

Transformer Primary Inductance
A flyback transformer needs to store substantial amounts of energy in the core during each switching cycle. The transformer, therefore, will generally require an air gap. The use of an air gap in the core makes the energy storage ability, or inductance, much more stable with temperature and variations in the core material. Most core manufacturers will supply standard sizes of air gaps with a given type of core, resulting in different AL values. AL is the inductance of a particular core per square turns of winding. To get a certain inductance, simply divide the desired inductance by the AL value and take the square root of the result to find the number of turns needed on the primary of the transformer.
The AP1458EQ detect the output voltage via the flyback pulse. Since this can only occur while the power switch is off, an important criteria is that the value of the primary inductance of the transformer be larger than a certain minimum value. **The switch off time should be 400ns or larger.** The minimum inductance can be calculated with the following formula:

$$Lpri \geq \frac{400 \cdot 10^{-9} \cdot DesiredOutputVoltage}{N \cdot DesiredIPEAK}$$

N: Transformer Turns Ratio

Transformer Leakage Inductance
The leakage inductance of the transformer must be carefully minimized for both proper and efficient operation of the part.

Transformer Secondary Capacitance
The total capacitance of the secondary should be minimized for both efficient and proper operation of the AP1458EQ. Since the secondary of the transformer under-goes large voltage swings any capacitance on the secondary can severely affect the efficiency of the circuit. In addition, the effective capacitance on the primary is largely dominated by the actual secondary capacitance. This is simply a result of any secondary capacitance being multiplied by N^2 when reflected to the primary. Since N is generally 10 or higher, a small capacitance of 10pF on the secondary is 100 times larger, or 1.0nF, on the primary. This capacitance forms a resonant circuit with the primary leakage inductance of the transformer. As such, both the primary leakage inductance and secondary side capacitance should be minimized.

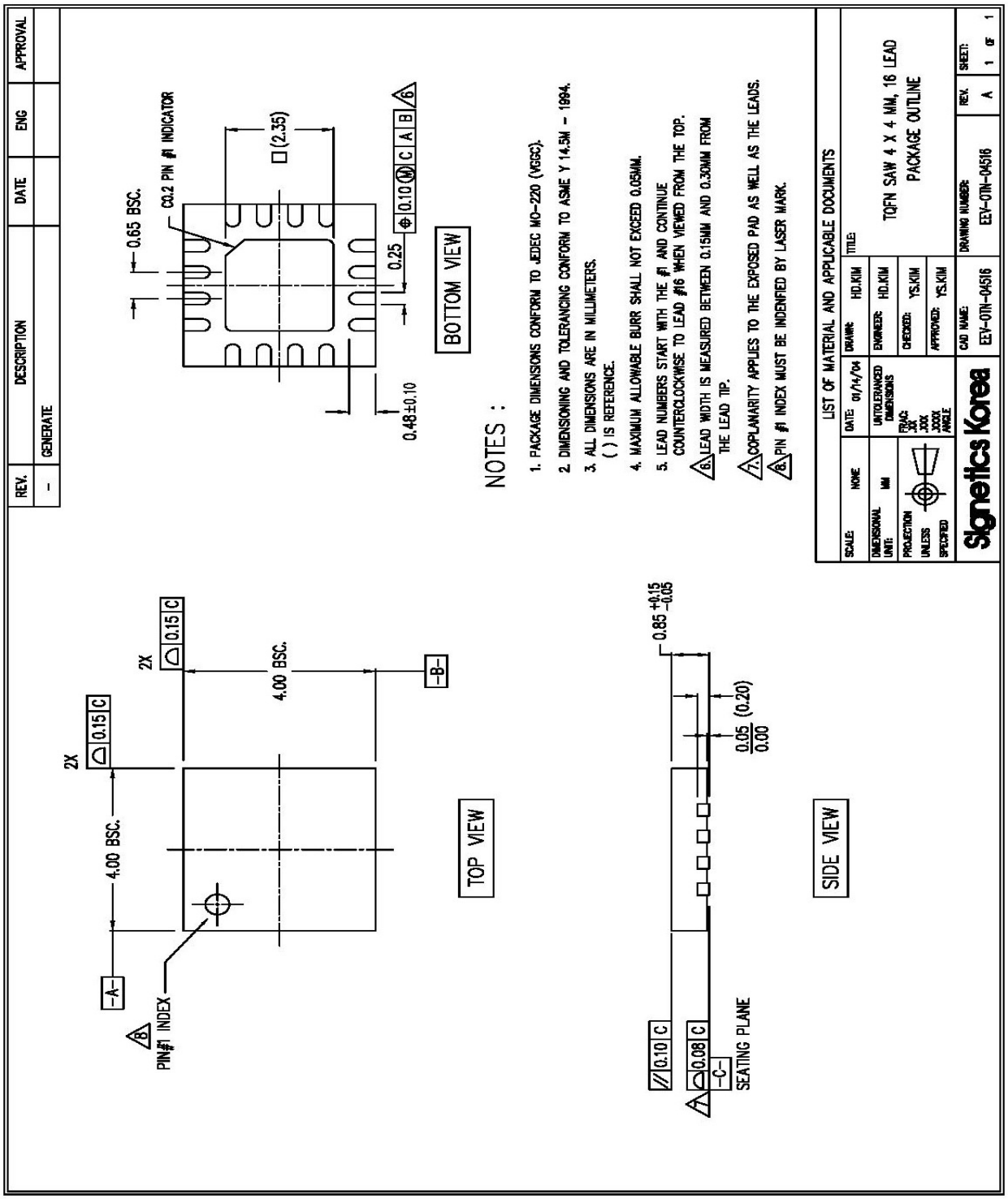
Capacitor Selection
The VBAT and VCC decoupling capacitors should be multilayer ceramic type with X5R or X7R dielectric. This insures adequate decoupling across wide ambient temperature ranges. Avoid Y5V or Z5U dielectrics.
Capacitor values depends from quality of supply sources. Tupical values are Cvcc=4.7μF, Cvbat=10μF.

Board Layout
The high voltage operation of the AP1458EQ demands careful attention to board layout. You will not get advertised performance with careless layout. Please keep all wires as short as possible. The board layout should be made with care for minimizing the parasitics. Figure below shows the recommended component placement. Keep the area for the high voltage end of the secondary as small as possible. Note the larger than minimum spacing for all high voltage nodes. This is necessary to meet the breakdown specifications for the circuit board. If the Photoflash capacitor is placed far from the AP1458EQ circuit, place a small (20nF-50nF) ceramic capacitor with sufficient voltage rating close to the part. This insures adequate bypassing. Remember that LETHAL VOLTAGES ARE PRESENT in this circuit. Use caution when working with the circuit.
To care of may be the problem comes from any parasitic capacitances between VPRIM and RREF.
Please try to minimize them:
VPRIM,RFB and RREF PCB lines should be distanced.
VPRIM,RFB and RREF PCB lines should be as short as possible.
RFB and RREF should be SMD components.

Rectifier Diode
Type: high voltage ultra fast recovery diode , Trr smaller is better performance (D = MMBT3004S)

$$V_{R\_\min} = V_{FL\_\max} + V_{Bat\_\max} \cdot U$$

13. TQFN16 Package Outlines



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