GaAs IC 75 Ω Non-Reflective SPDT Switch 0.5–2 GHz

SKYWORKS

AS163-73

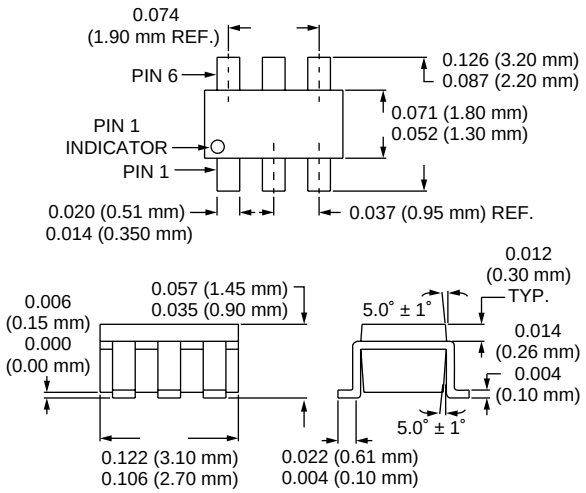
Features

- 75 Ω Impedance
- Positive Control Voltage
- Non-Reflective
- Low DC Power Consumption
- Small Low Cost SOT-6 Plastic Package

Description

The AS163-73 is an IC FET non-reflective SPDT switch in a low cost SOT-6 plastic package. The AS163-73 features low insertion loss and positive voltage operation with very low DC power consumption. This general purpose switch can be used in a variety of CATV applications.

SOT-6



Electrical Specifications at 25°C (0, +3 V)

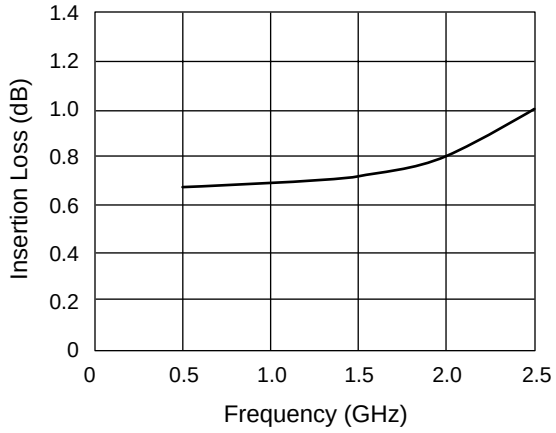
Parameter[1]	Frequency	Min.	Typ.	Max.	Unit
Insertion Loss[2]	0.5–1.0 GHz 0.5–2.0 GHz		0.7 0.8	0.9 1.0	dB dB
Isolation	0.5–1.0 GHz 0.5–2.0 GHz	33 27	37 30		dB dB
VSWR[3]	0.5–1.0 GHz 0.5–2.0 GHz		1.7:1 1.4:1	2.0:1 1.5:1	

Operating Characteristics at 25°C (0, +3 V)

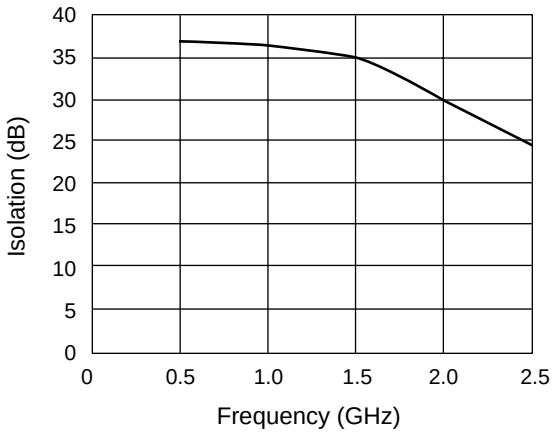
Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Switching Characteristics[4]	Rise, Fall (10/90% or 90/10% RF) On, Off (50% CTL to 90/10% RF) Video Feedthru			10 20 25		ns ns mV
Input Power for 1 dB Compression	0/+3 V 0/+5 V	0.5–2.0 GHz 0.5–2.0 GHz		+21 +28		dBm dBm
Intermodulation Intercept Point (IP3)	For Two-tone Input Power +13 dBm	0.5–2.0 GHz		+45		dBm
Control Voltages	V_{Low} = 0 to 0.2 V @ 20 µA Max. V_{High} = +3 V @ 100 µA Max. to +5 V @ 200 µA Max. $V_S = V_{High} \pm 0.2$ V					

1. All measurements made in a 75 Ω system, unless otherwise specified.
2. Insertion loss changes by 0.003 dB/°C.
3. Insertion loss state.
4. Video feedthru measured with 1 ns risetime pulse and 500 MHz bandwidth.

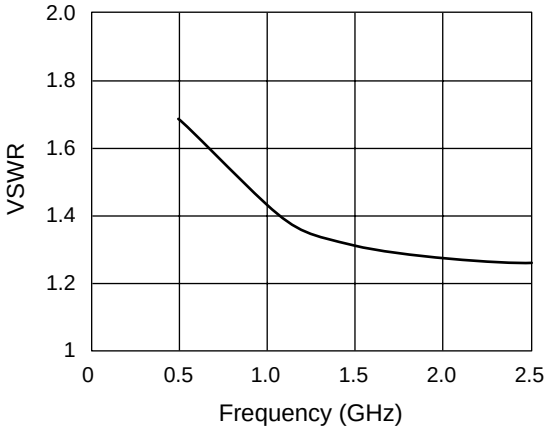
Typical Performance Data (0, +3 V) @ 75 Ω



Insertion Loss vs. Frequency



Isolation vs. Frequency



VSWR vs. Frequency

Absolute Maximum Ratings

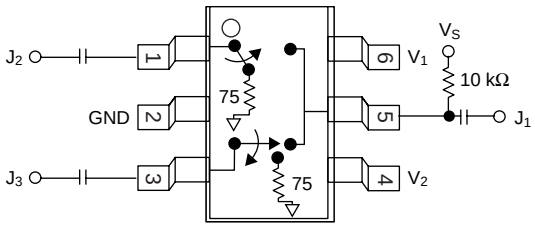
Characteristic	Value
RF Input Power	2 W > 500 MHz 0/+7 V Control
Control Voltage	-0.2 V, +8 V
Operating Temperature	-40°C to +85°C
Storage Temperature	-50°C to +150°C
Θ_{JC}	25°C/W

Truth Table

V_1	V_2	J_1–J_2	J_1–J_3
V_{High}	0	Insertion Loss	Isolation
0	V_{High}	Isolation	Insertion Loss

V_{High} = +3 to +5 V (V_S = V_{High} ± 0.2 V).

Pin Out



DC blocking capacitors (C_{BL}) and biasing resistor must be supplied externally for positive operation.
C_{BL} = 100 pF for operation >500 MHz.