

# CXA3691AEN

### Description

The CXA3691AEN is a high-speed buffer amplifier IC.  
(Applications: CCD image sensor output buffers, Digital still cameras, Camcorders, Other general buffers)

### Features

- ◆ Power consumption: 24mW (typ.)  
(IDRV = 50 $\mu$ A (220k $\Omega$  when V<sub>CC</sub> = 15V), ISF pin connected to GND, during no signal)
- ◆ Push-pull output
- ◆ High-speed response: 500V/ $\mu$ s (IDRV = 50 $\mu$ A (220k $\Omega$  when V<sub>CC</sub> = 15V), C<sub>L</sub> = 20pF)
- ◆ Internal sink current mode for CCD with open source output  
(Settable by external resistance R<sub>ISF</sub>)
- ◆ Enables to set the responsibility by changing the drive current by an external resistor

### Structure

Bipolar silicon monolithic IC

### Absolute Maximum Ratings

(T<sub>a</sub> = 25°C)

◆ Supply voltage	V <sub>CC</sub>	16	V
◆ Supply voltage	I <sub>N</sub>	GND – 0.3 to V <sub>CC</sub> + 0.3	V
◆ Storage temperature	T <sub>stg</sub>	–65 to +150	°C
◆ Allowable power dissipation	P <sub>D</sub>	0.28	W

(when mounted on a two-layer board; 50mm × 50mm, t = 1.6mm)

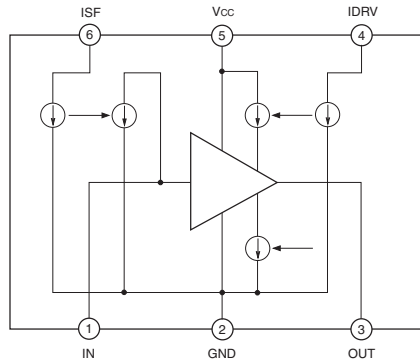
### Recommended Operating Conditions

◆ Supply voltage	V <sub>CC</sub>	9.0 to 15.5	V
◆ Operating temperature	T <sub>a</sub>	–20 to +75	°C

Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

Block Diagram and Pin Configuration

(Top View)



Pin Description and I/O Pin Equivalent Circuit

Pin No.	Symbol	I/O	Standard voltage level	Equivalent circuit	Description
2	GND	—	0V	—	GND.
5	Vcc	—	15V	—	Supply voltage input.
1	IN	I	CCD output voltage		Input.
6	ISF	I	—		External resistor connection for setting the sink current for CCD with open source output. Connect an external resistor between this pin and Vcc (Pin 5). Connect this pin to GND (Pin 2) when not using this function. * The minimum value of the external resistance should be 100kΩ (when Vcc = 15V).
3	OUT	O	≈IN		Output.
4	IDRV	I	—		External resistor connection for setting the drive current. Connect an external resistor between this pin and Vcc (Pin 5). * The minimum value of the external resistance should be 100kΩ (when Vcc = 15V).

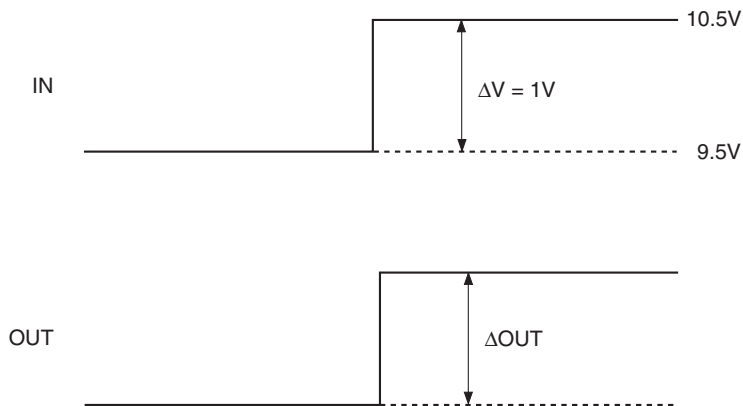
**Electrical Characteristics**

(Ta = 25°C, VCC = 15V, RIDRV = 220kΩ, ISF pin: connected to GND)

**DC Characteristics**

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Supply current	ICC	IN = 10V, RIDRV = 220kΩ	1.4	1.6	1.8	mA
Voltage gain	VGAIN	*1 IN: 10Vdc ΔV = 1V GAIN = ΔOUT/ΔV	—	0.999	—	V/V
I/O offset voltage	VOFFSET	IN = 10V VOFFSET = OUT-IN	-100	—	100	mV
I/O voltage range	VRANGE	RIDRV = 100kΩ RIDRV = 150kΩ RIDRV = 220kΩ RIDRV = 330kΩ	3.3 2.9 2.5 2.1	— — — —	VCC - 2.0 VCC - 1.85 VCC - 1.8 VCC - 1.7	V
Input bias current	IBIAS	IN = 10V, ISF = 0V	-15	-5	6	μA
Sync current	ISINK	IN = 10V, RISF = 220kΩ	2.6	2.9	3.2	mA

\*1 Voltage gain

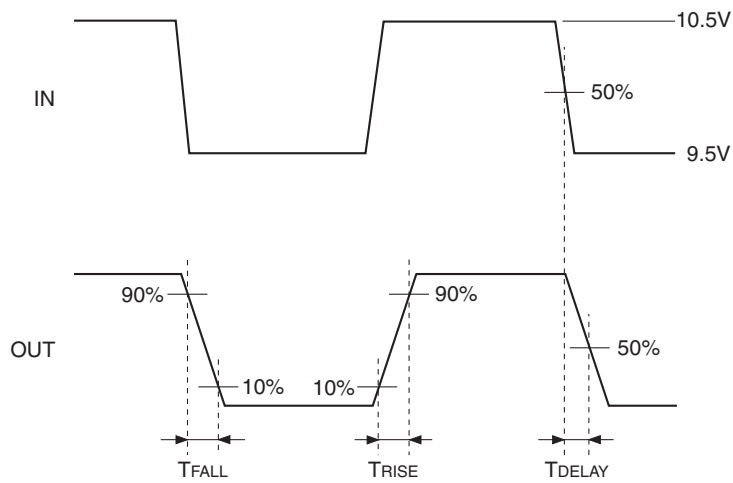


**AC Characteristics**

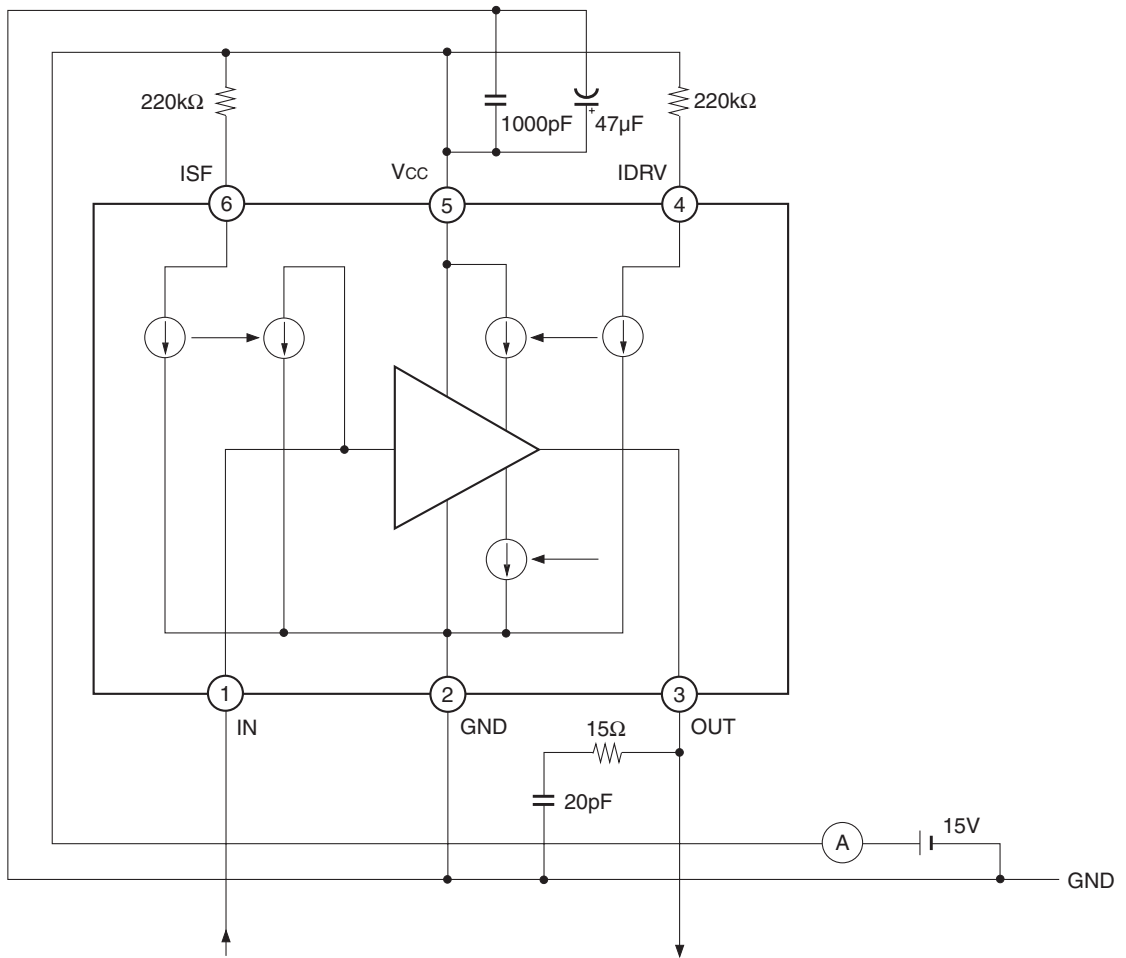
( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 15\text{V}$ ,  $I_{DRV} = 50\mu\text{A}$  (220k $\Omega$  when  $V_{CC} = 15\text{V}$ ), ISF pin: connected to GND,  $R_L = 15\Omega$ ,  $C_L = 20\text{pF}$ )

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Bandwidth	GBW	IN = 50mVp-p	—	220	—	MHz
Rise time	T <sub>RISE</sub>	*1 IN = 9.5 to 10.5V 10 to 90%	—	2.5	3.5	ns
Fall time	T <sub>FALL</sub>	*1 IN = 10.5 to 9.5V 10 to 90%	—	3.0	4.0	ns
I/O delay time	T <sub>DELAY</sub>	*1 IN = 9.5 to 10.5V @50%	0.9	1.0	2.0	ns

\*1 Rise time, fall time and I/O delay time



Evaluation Circuit



## Description of Operation

### Current Settings

#### 1. Output Drive Current

The small signal output impedance of the OUT pin (Pin 3) can be set by connecting the IDR pin (Pin 4) to  $V_{CC}$  through a resistor. The inflow current to the IDR pin is multiplied by 10 times inside the IC, and flows as the output stage idling current.

The IDR pin has an internal  $50\text{k}\Omega$  resistor, so the inflow current to the IDR pin can be calculated as follows.

$$\begin{aligned} I_{IDR} &= (V_{CC} - V_{BE} \times 2) / (R_{IDR} + 50\text{k}\Omega) \\ &= (15 - 1.46) / 270\text{k}\Omega \\ &= 50.1\mu\text{A} \end{aligned}$$

Here,  $V_{CC} = 15\text{V}$ ,  $V_{BE} = 0.73\text{V}$  (typ.), and  $R_{IDR} = 220\text{k}\Omega$ .

The small signal output impedance at this time can be calculated as follows.

$$\begin{aligned} R_{OUT} &= (26\text{mV} / (10 \times I_{IDR})) / 2 \\ &= (26\text{mV} / 501\mu\text{A}) / 2 \\ &= 26\Omega \end{aligned}$$

#### 2. Sink Current for CCD with open source output

The sink current of the IN pin (Pin 6) can be set by connecting the ISF pin (Pin 1) to  $V_{CC}$  through a resistor. This sink current can be used as the CCD output stage source follower drive current. The inflow current to the ISF pin is multiplied by 58 times inside the IC, and flows as the sink current.

The ISF pin has an internal  $50\text{k}\Omega$  resistor, so the inflow current to the ISF pin can be calculated as follows.

$$\begin{aligned} I_{ISF} &= (V_{CC} - V_{BE} \times 2) / (R_{ISF} + 50\text{k}\Omega) \\ &= (15 - 1.46) / 270\text{k}\Omega \\ &= 50.1\mu\text{A} \end{aligned}$$

Here,  $V_{CC} = 15\text{V}$ ,  $V_{BE} = 0.73\text{V}$  (typ.), and  $R_{ISF} = 220\text{k}\Omega$ .

The sink current at this time can be calculated as follows.

$$\begin{aligned} I_{\text{sink}} &= 58 \times I_{ISF} \\ &= 2.9\text{mA} \end{aligned}$$

Note) This IC operation depends on IDR and ISF.

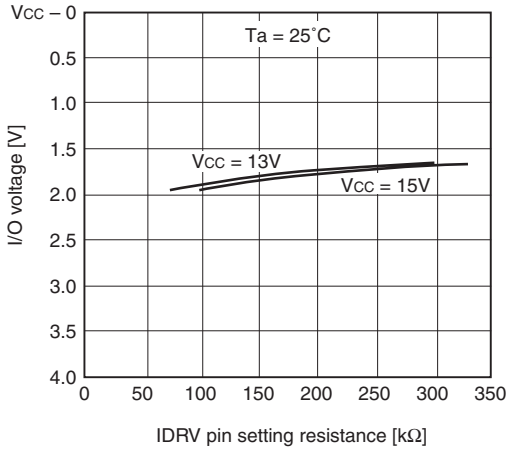
This specification is described based on IDR of  $220\text{k}\Omega$  when  $V_{CC} = 15\text{V}$ . However, set it to  $180\text{k}\Omega$  to occur the same current when using under the condition that  $V_{CC} = 13\text{V}$ .

[IDR and ISF vs external resistor]

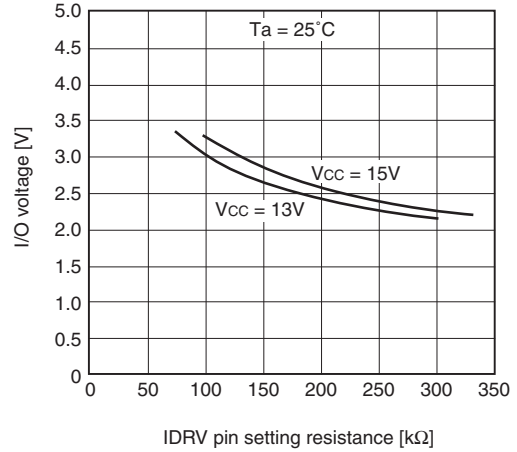
Current ( $\mu\text{A}$ )	90	68	50	35	26	Unit
When $V_{CC} = 15\text{V}$	100	150	220	330	470	$\text{k}\Omega$
When $V_{CC} = 13\text{V}$	78	120	180	270	390	$\text{k}\Omega$

Example of Representative Characteristics

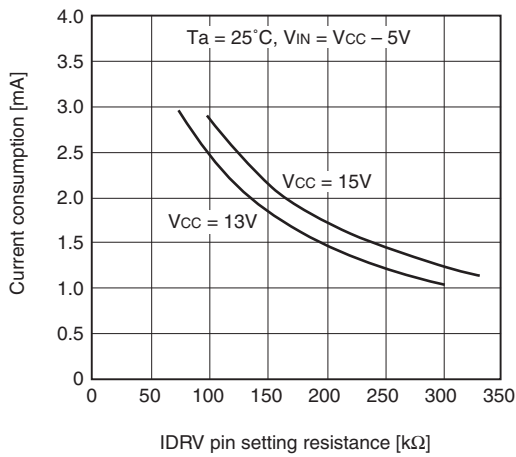
(Upper side) I/O voltage range vs. IDRV pin setting resistance



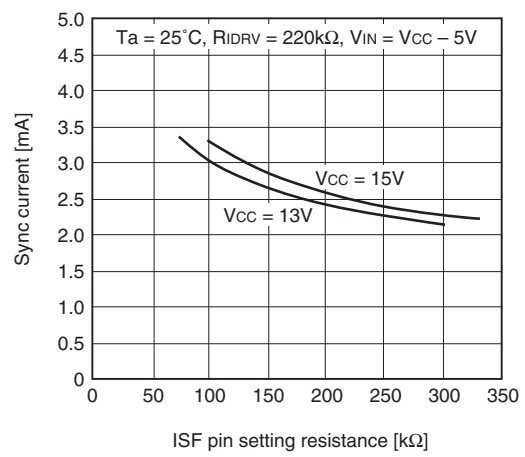
(Lower side) I/O voltage range vs. IDRV pin setting resistance



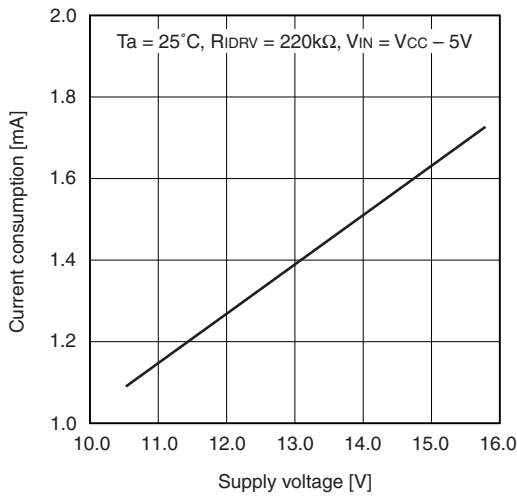
Current consumption vs. IDRV pin setting resistance



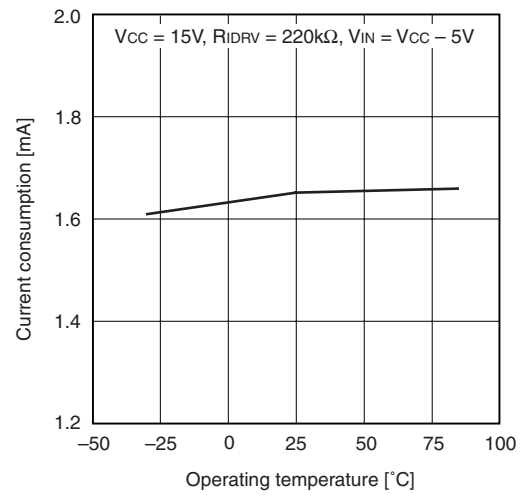
Sink current vs. ISF pin setting resistance

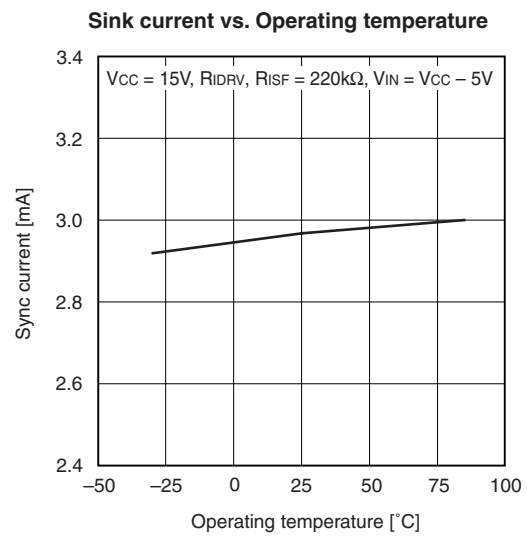
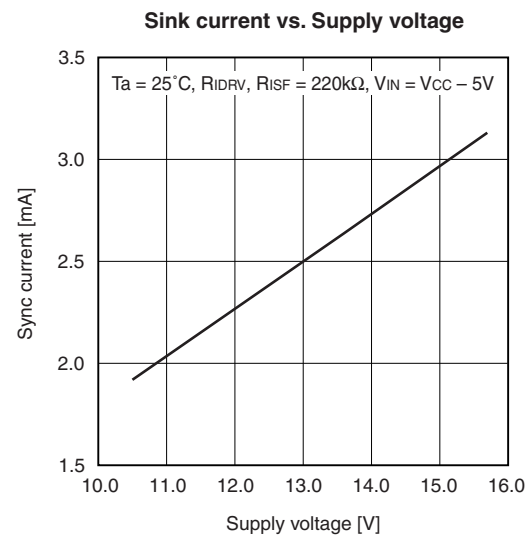
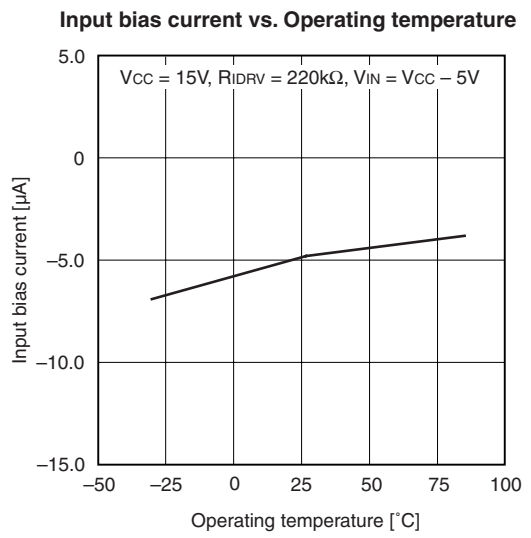
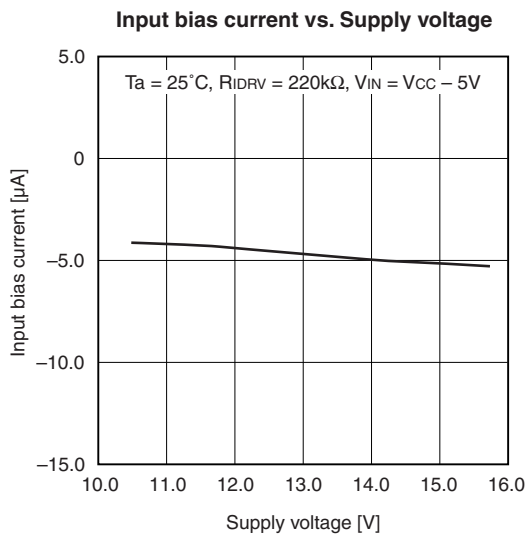
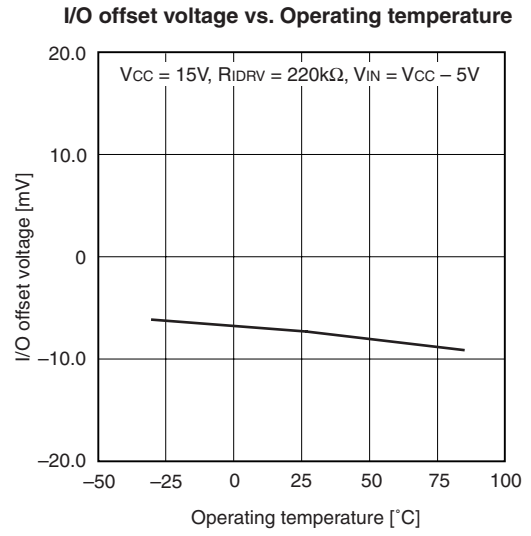
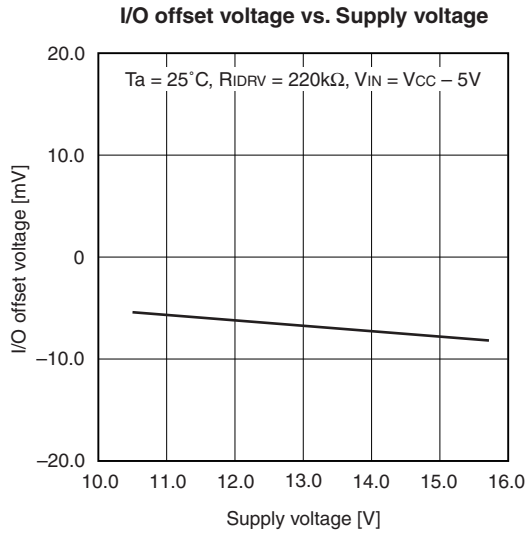


Current consumption vs. Supply voltage



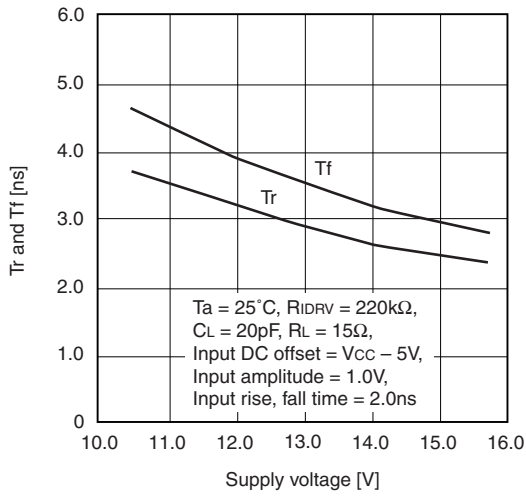
Current consumption vs. Operating temperature



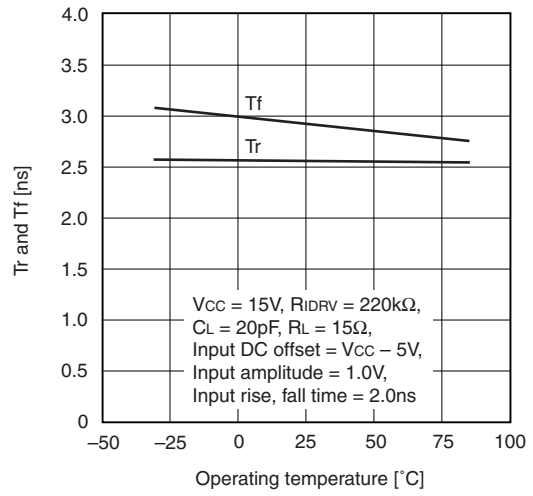




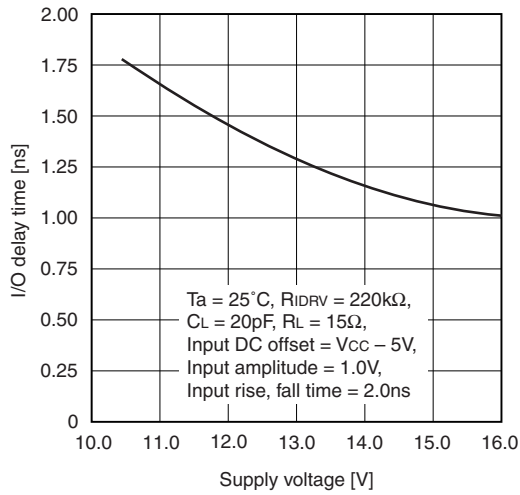
**Tr and Tf vs. Supply voltage**



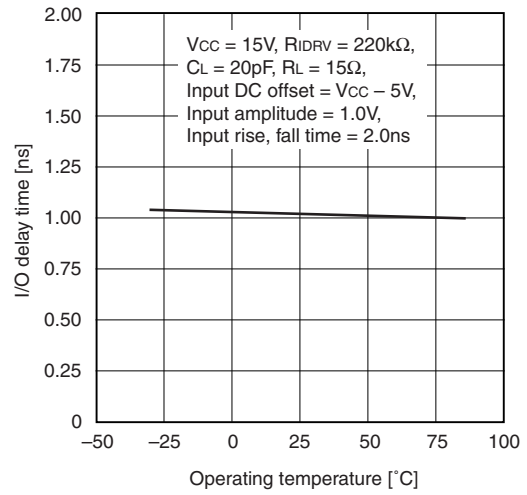
**Tr and Tf vs. Operating temperature**



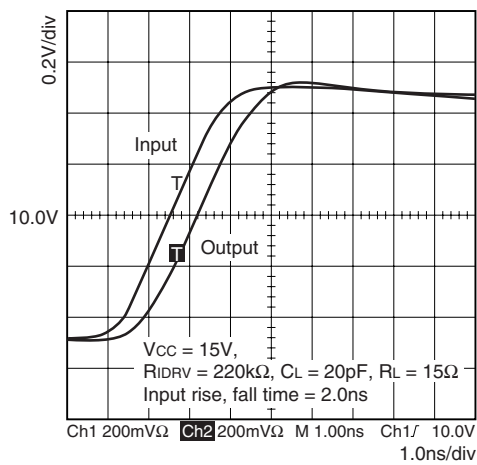
**I/O delay time vs. Supply voltage**



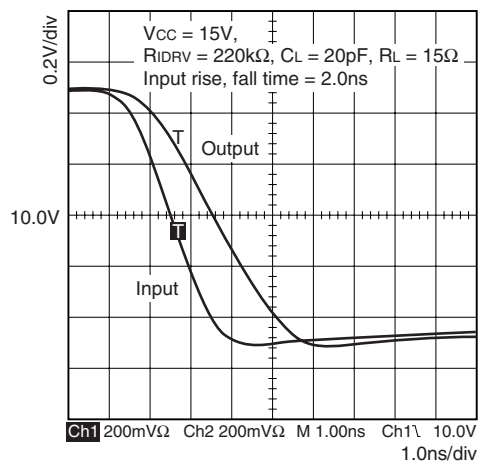
**I/O delay time vs. Operating temperature**



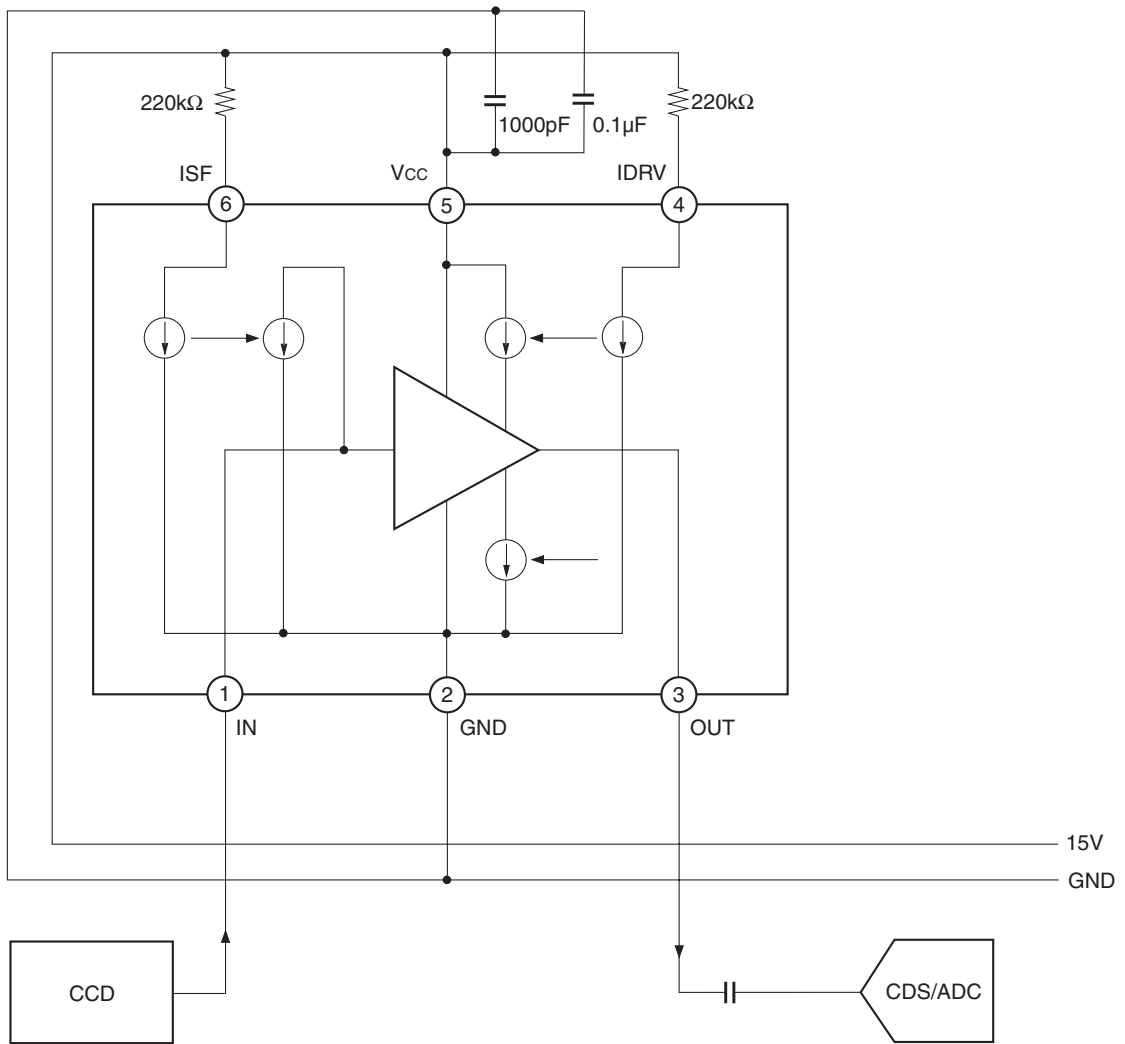
**Positive pulse response**



**Negative pulse response**

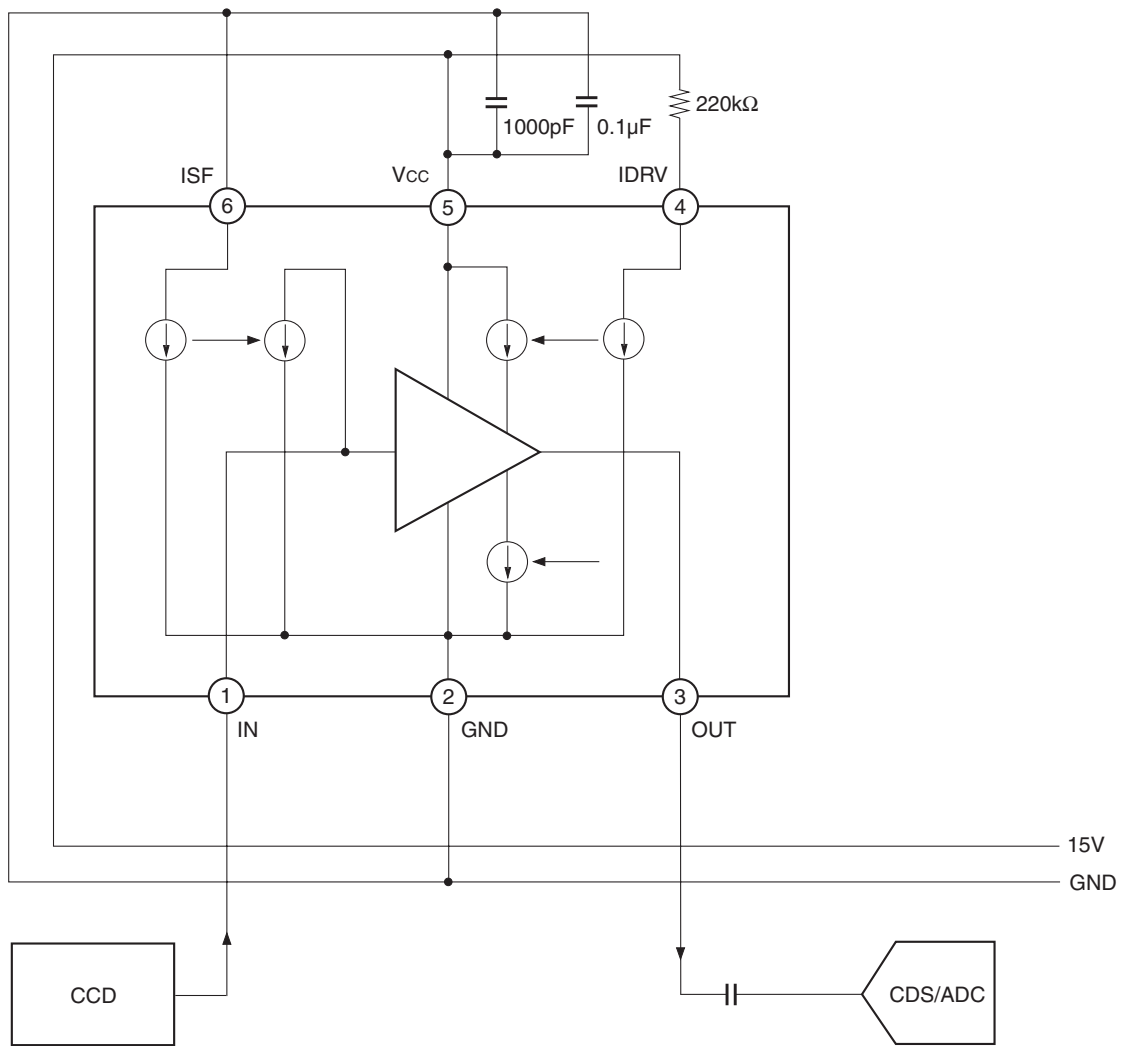


Application Circuit 1 (when using CCD with open source output )



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit 2 (when using CCD with internal current source)



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

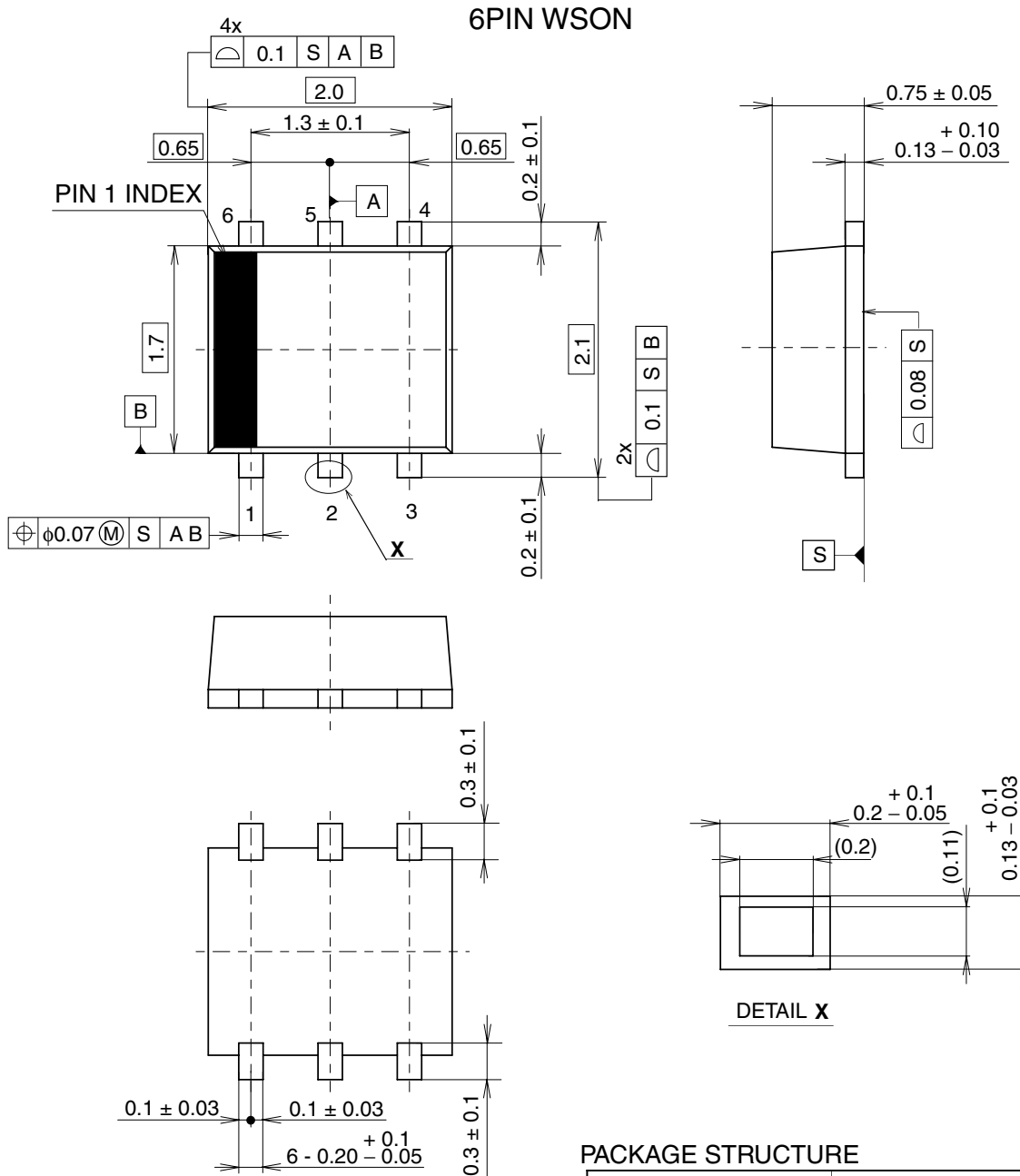


## Notes on Operation

- ◆ Provide the widest GND pattern possible on the board.
- ◆ Use a 1000pF (recommended) and a 0.1 $\mu$ F (recommended) ceramic capacitors in parallel for the bypass capacitor connected between the power supply and GND, and connect them as close to the IC pins as possible.
- ◆ Load capacitance causes the input/output wiring response to worsen and results in noise. Use the shortest wiring layout possible, and shield it with GND.
- ◆ When the output pin (Pin 3) is shorted to either the power supply or GND, an overcurrent may flow to the output stage elements and damage them.  
When the input pin (Pin 1) is shorted to GND, an overcurrent may flow to the internal parasitic elements and damage them.

Package Outline

(Unit: mm)



SONY CODE	WSON-6P-051
EIAJ CODE	_____
JEDEC CODE	_____

**PACKAGE STRUCTURE**

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	Sn-Bi
TERMINAL MATERIAL	COPPER
PACKAGE MASS	0.008g

**LEAD PLATING SPECIFICATIONS**

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18µm