YAMAHA

YDA158

D-4HP2

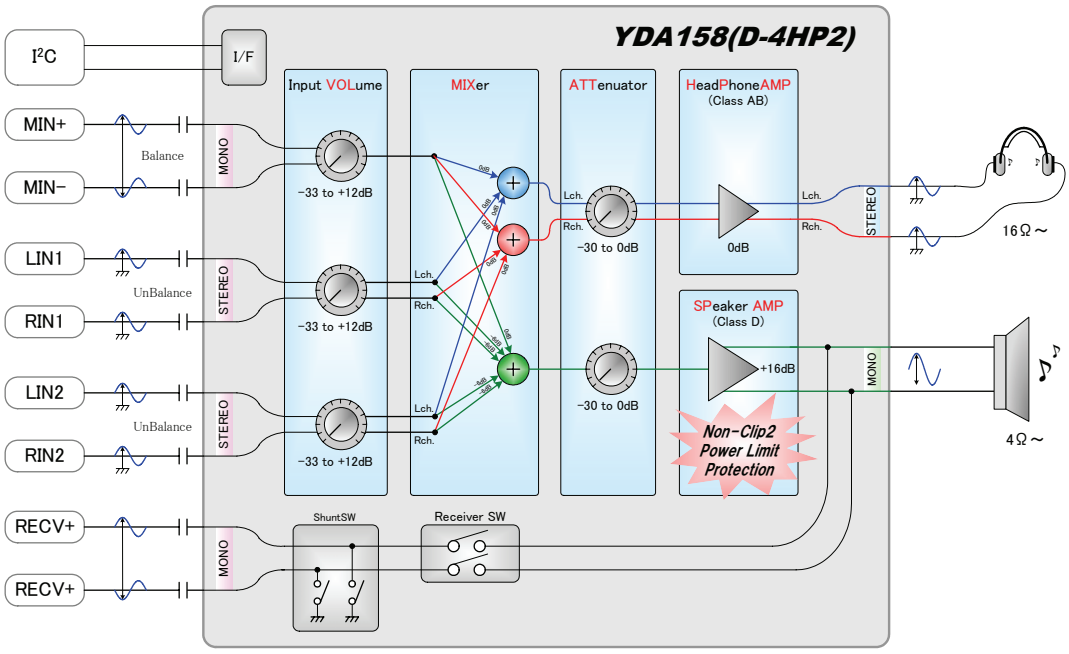
MONAURAL 2.6W Non-Clip DIGITAL AUDIO POWER AMPLIFIER

■ Outline

The YDA158 (D-4HP2) is a 2.6W (R_L=4Ω)×1ch Class-D amplifier with a capless stereo headphone amplifier and receiver output. Its superior sound quality, the lowest level of distortion and noise are achieved by “Pure Pulse Direct Speaker Drive Circuit” which does not need a number of components such as a LC filter.

The YDA158 features "Non-Clip2" and “Power Limit” circuits which were developed by Yamaha. The circuits automatically detect and prevent clipping noise by shortage of supply voltage. Moreover, it is possible to set the THD level to control sound pressure.

The YDA158 has the I^2C interface to control input volume, mixer, output level attenuator, power-down mode, etc. In addition, the protect function (over current, high temperature, low supply voltage malfunction), the pop noise reduction, the EMI noise reduction and the superior PSRR against TDMA (GSM) are equipped.



Schematic Diagram

■ Features

- Power Supply: V_{SPVDD} 2.7V (2.6V : min.-30°C) to 5.25V; V_{AVDD}, V_{HPVDD} 2.7V (2.6V : min.-30°C) to 3.3V
- Input: Mono (balance) × 1, Stereo (unbalance) × 2
- Output: Monaural Speaker (PWM, BTL) × 1, Stereo Headphone (class AB, SEPP) × 1

Speaker Amplifier (monaural)

- Maximum Continuous Output
  - 2.6 W×1ch* (V_{SPVDD}=5.0V, R_L=4Ω, THD+N=10%, 25°C)
  - 0.8 W×1ch* (V_{SPVDD}=3.6V, R_L=8Ω, THD+N=10%, 25°C)
- Maximum Momentary Output
  - 2.6 W×1ch (V_{SPVDD}=5.0V, R_L=4Ω, THD+N=10%)
  - 2.2 W×1ch (V_{SPVDD}=5.0V, R_L=4Ω, THD+N=1%)
  - 0.8 W×1ch (V_{SPVDD}=3.6V, R_L=8Ω, THD+N=10%)
  - 0.68 W×1ch (V_{SPVDD}=3.6V, R_L=8Ω, THD+N=1%)
- Distortion (THD+N) 0.045 % (V_{SPVDD}=3.6V, R_L=8Ω, Po=0.4W, 1kHz)
- Residual Noise 40μVrms (V_{SPVDD}=3.6V, Mute)
- S/N Ratio 90 dB (V_{SPVDD}=3.6V, Vout: THD+N=10%)
- Efficiency 84 % (V_{SPVDD}=3.6V, R_L=8Ω, Po=0.8W); 75 % (V_{SPVDD}=3.6V, R_L=8Ω, Po=0.1W)
- EMI Noise Reduction
- TDMA(GSM) High PSRR= -75dB (V_{SPVDD} 3.6V, 217Hz)
- Non-Clip2 (THD ≤1%, 3%, 5%, 8%, 10%)
- Non-Clip2 Attack Time/Release Time Setting Function
- Power Limit (0.39, 0.47, 0.60, 0.78, 0.90, 1.10W@8Ω)
- Receiver Output Function (RECV/Speaker Amplifier Selectable Output)
- Overcurrent Protection Function
- High Temperature Protection Function

Capless Headphone Amplifier (stereo)

- Maximum Continuous Output
  - 30mW×2ch (WLCSP, V_{HPVDD}=3.0V, R_L=16Ω,THD+N=1%)
  - 27mW×2ch (QFN, V_{HPVDD}=3.0V, R_L=16Ω,THD+N=1%)
- Distortion (THD+N) 0.03 % (V_{HPVDD}=3.0V, R_L=16Ω, Po=5mW, 1kHz)
- Residual Noise 10μVrms (V_{HPVDD}=3.0V, Mute)
- S/N Ratio 92 dB (V_{HPVDD}=3.0V, R_L=16Ω, Vout: THD+N=1%)

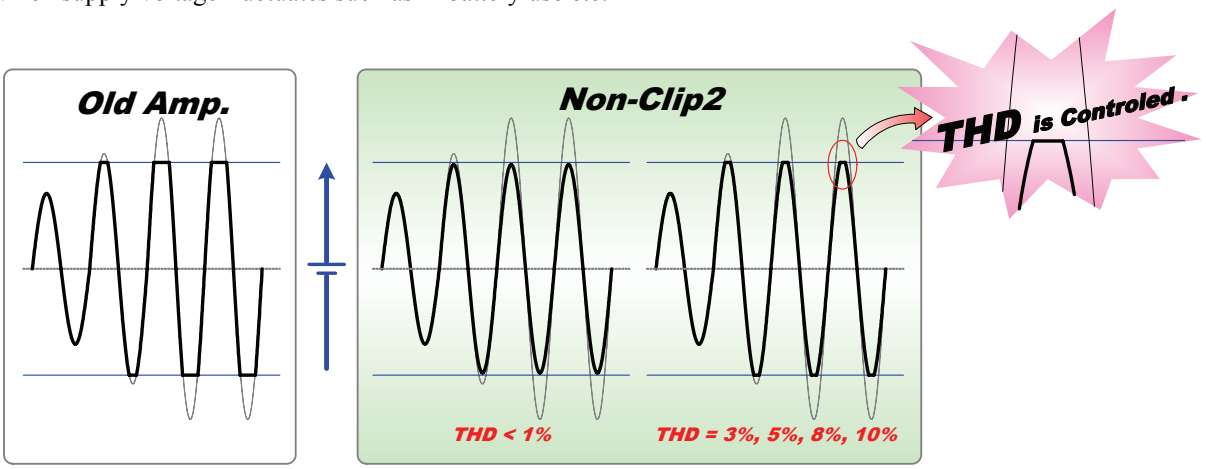
Common

- Input Volume (-33 to +12dB/1.5dB Step)
- Mixing Function
- Output Attenuator (-30 to 0dB/1.0dB Step)
- High-speed Startup
- Pop Noise Reduction
- Power-down Function
- I^2C Control
- Low-voltage Malfunction Prevention Function
- Lead-free Package 30 balls WLCSP (YDA158-PZ); 32 pins QFN (YDA158-QZ)

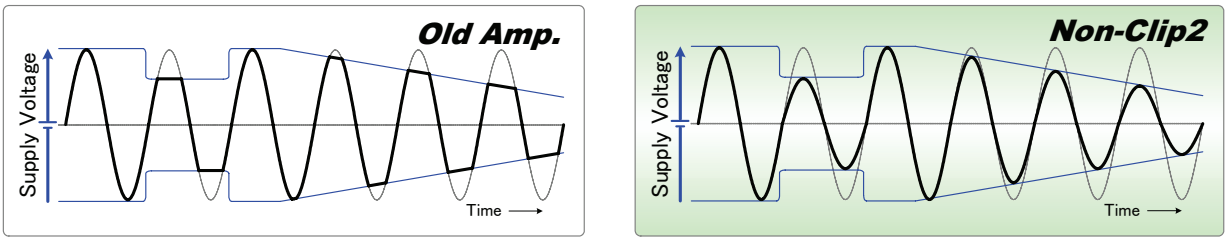
* θja＝28°C/W (Conditions: WLCSP Evaluation Board (4 layers), no wind)

■ Non-Clip 2 Function

This is the function to control the speaker output clipped to a supply voltage by automatically controlling PWM amplifier gain so that it may not be distorted. Furthermore, it is also possible to set the amount of distortion such as THD=10%, etc. Since this function always follows the supply voltage, it also exerts an effect on the case in which supply voltage fluctuates such as in battery use etc.

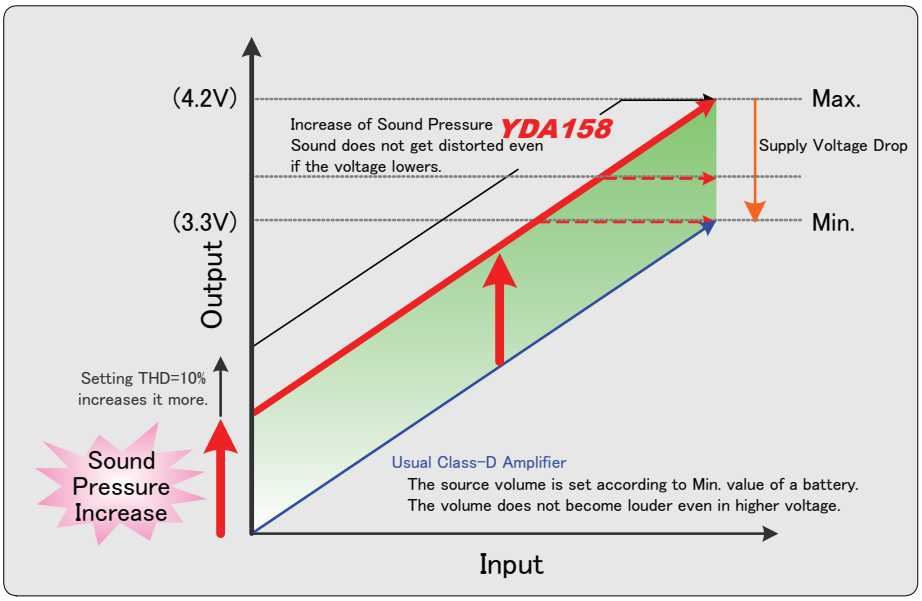


Non-Clip 2 Conceptional Diagram



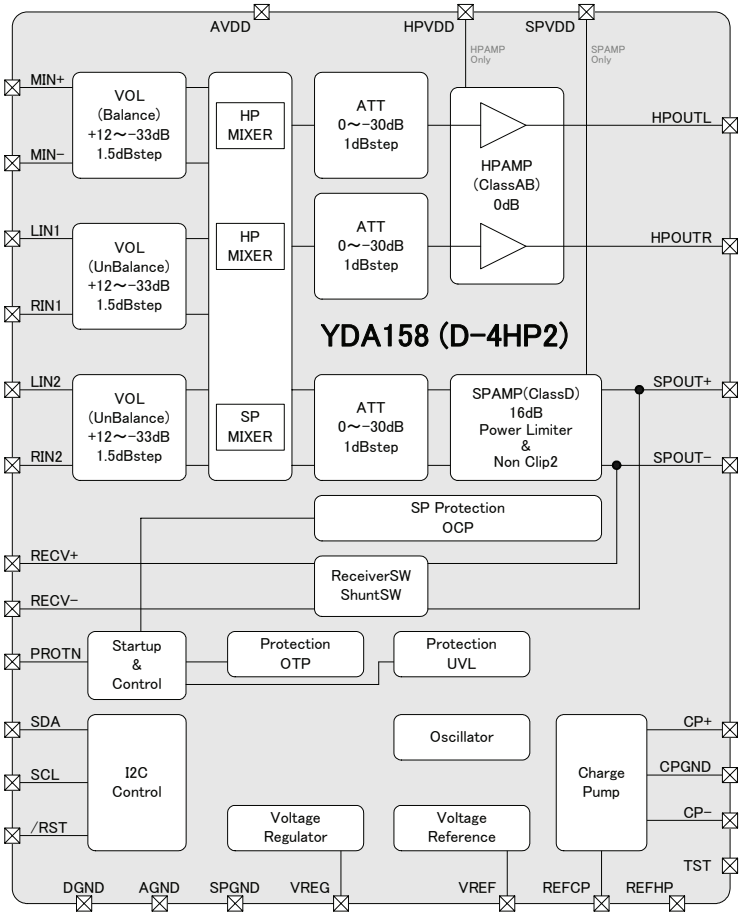
Following for the change of the supply voltage

In a conventional way, when there is a possibility of fluctuation of the supply voltage, source's volume is set so that the output does not get distorted based on the minimum voltage. But, with Non-Clip2, a source volume can be set on the basis of the maximum voltage because it always controls the volume automatically.
This is an ideal function for an application that requires much sound pressure because this allows increasing the total sound pressure level.



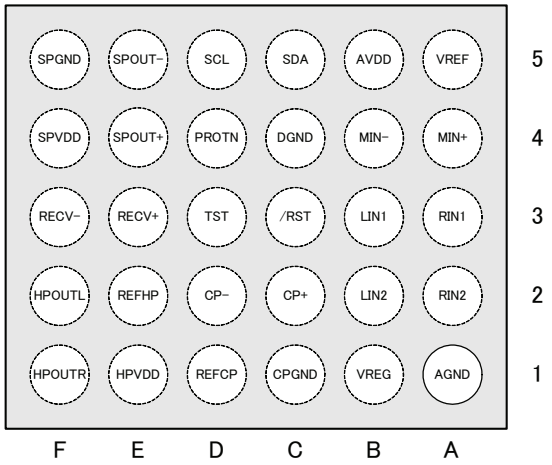
Non-Clip2 Sound Pressure Increase

■ Block Diagram

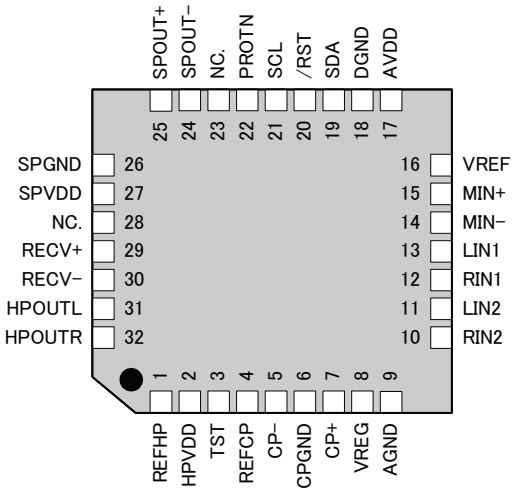


Block Diagram

■ Pin Arrangement



30-balls WLCSP (Bottom View)



32-pin QFN (Top View)

■ Pin Function (WLCSP)

WLCSP Pin Function

No.	Name	I/O	Protection Circuit	Function
A1	AGND	GND	—	Ground for Analog Circuit
A2	RIN2	A	P,N	Stereo Input Pin 2 (Rch.) (*1)
A3	RIN1	A	P,N	Stereo Input Pin 1 (Rch.) (*1)
A4	MIN+	A	P,N	Monaural Differential Input Pin (positive) (*1)
A5	VREF	A	P,N	Analog Reference Power Supply Pin
B1	VREG	O	—	Reference Voltage Pin
B2	LIN2	A	P,N	Stereo Input Pin 2 (Lch.) (*1)
B3	LIN1	A	P,N	Stereo Input Pin 1 (Lch.) (*1)
B4	MIN-	A	P,N	Monaural Differential Input Pin (negative) (*1)
B5	AVDD	Power	—	Analog Power Supply
C1	CPGND	GND	—	Ground for Charge Pump
C2	CP+	O	—	Charge Pump pin (positive)
C3	/RST	IS	N	Reset Pin, "L": Reset
C4	DGND	GND	—	Digital Ground
C5	SDA	IOD	N	I^2C Serial Data Pin
D1	REFCP	O	—	Charge Pump Output Pin
D2	CP-	O	—	Charge Pump pin (negative)
D3	TST	IS	N	Test setting Pin (Ground Connection)
D4	PROTN	OD	—	Error Output Pin (overcurrent, high temperature)
D5	SCL	IS	N	I^2C Serial Clock Pin
E1	HPVDD	Power	—	Power Supply for Headphone Amplifier
E2	REFHP	A	N	Minus Reference Voltage Pin for Headphone Amplifier
E3	RECV+	A	N	Receiver Signal Input Pin (positive) (*2)
E4	SPOUT+	O	—	Speaker Amplifier Output Pin (positive)
E5	SPOUT-	O	—	Speaker Amplifier Output Pin (negative)
F1	HPOUTR	O	—	Headphone Amplifier Output Pin (Rch.)
F2	HPOUTL	O	—	Headphone Amplifier Output Pin (Lch.)
F3	RECV-	A	N	Receiver Signal Input Pin (negative) (*2)
F4	SPVDD	Power	—	Power Supply for Speaker Amplifier Output
F5	SPGND	GND	—	Ground for Speaker Amplifier Output

A: Analog Pin, IS: Schmitt Trigger Input Pin, O: Output Pin, OD: Open-drain Pin, IOD: I/O Pin (Open-drain Output)

* 1. Note that leakage current flows through the protection circuit (PMOS Tr.) when applying a voltage higher than AVDD to this pin.
* 2. Note that leakage current flows when applying a voltage higher than SPVDD to this pin.

■ Pin Function (QFN)

QFN Pin Function

No.	Name	I/O	Protection Circuit	Function	
1	REFHP	A	N	Minus Reference Voltage Pin for Headphone Amplifier	
2	HPVDD	Power	—	Power Supply for Headphone Amplifier	
3	TST	IS	N	Test setting Pin (Ground Connection)	
4	REFCP	O	—	Charge Pump Output Pin	
5	CP-	O	—	Charge Pump pin (negative)	
6	CPGND	GND	—	Ground for Charge Pump	
7	CP+	O	—	Charge Pump pin (positive)	
8	VREG	O	—	Reference Voltage Pin	
9	AGND	GND	—	Ground for Analog Circuit	
10	RIN2	A	P,N	Stereo Input Pin 2 (Rch.)	(*1)
11	LIN2	A	P,N	Stereo Input Pin 2 (Lch.)	(*1)
12	RIN1	A	P,N	Stereo Input Pin 1 (Rch.)	(*1)
13	LIN1	A	P,N	Stereo Input Pin 1 (Lch.)	(*1)
14	MIN-	A	P,N	Monaural Differential Input Pin (negative)	(*1)
15	MIN+	A	P,N	Monaural Differential Input Pin (positive)	(*1)
16	VREF	A	P,N	Analog Reference Power Supply Pin	
17	AVDD	Power	—	Analog Power Supply	
18	DGND	GND	—	Digital Ground	
19	SDA	IOD	N	I^2C Serial Data Pin	
20	/RST	IS	N	Reset Pin, "L": Reset	
21	SCL	IS	N	I^2C Serial Clock Pin	
22	PROTN	OD	—	Error Output Pin (overcurrent, high temperature)	
23	NC.	—	—	—	
24	SPOUT-	O	—	Speaker Amplifier Output Pin (negative)	
25	SPOUT+	O	—	Speaker Amplifier Output Pin (positive)	
26	SPGND	GND	—	Ground for Speaker Amplifier Output	
27	SPVDD	Power	—	Power Supply for Speaker Amplifier Output	
28	NC.	—	—	—	
29	RECV+	A	N	Receiver Signal Input Pin (positive)	(*2)
30	RECV-	A	N	Receiver Signal Input Pin (negative)	(*2)
31	HPOUTL	O	—	Headphone Amplifier Output Pin (Lch.)	
32	HPOUTR	O	—	Headphone Amplifier Output Pin (Rch.)	

A: Analog Pin, IS: Schmitt Trigger Input Pin, O: Output Pin, OD: Open-drain Pin, IOD: I/O Pin (Open-drain Output)

* 1. Note that leakage current flows through the protection circuit (PMOS Tr.) when applying a voltage higher than AVDD to this pin.
* 2. Note that leakage current flows when applying a voltage higher than SPVDD to this pin.

■ Electrical Characteristics

Absolute Maximum Ratings See Note.)

Item	Symbol	Min.	Max.	Unit
SPVDD pin Voltage Range	V_{SPVDD}	-0.3	6.0	V
AVDD pin Voltage Range	V_{AVDD}	-0.3	4.2	V
HPVDD pin Voltage Range	V_{HPVDD}	-0.3	4.2	V
Input pin Voltage Range (Analog input pins) *1	V_{INA}	V_{AGND}−0.6	V_{AVDD} +0.6	V
Input pin Voltage Range (RECV+,RECV- pins)	V_{INR}	V_{SPGND}−0.3	V_{SPVDD} +0.3	V
Input pin Voltage Range (input pins other than the above)	V_{IN}	V_{AGND}−0.3	V_{AVDD} +0.3	V
Power Dissipation (WLCSP30,Ta=25℃) *2	P_{D25}	-	3.54	W
Power Dissipation (WLCSP30,Ta=70℃) *2	P_{D70}		1.95	
Power Dissipation (WLCSP30,Ta=85℃) *2	P_{D85}		1.42	
Power Dissipation (QFN32,Ta=25℃) *3	P_{D25}	-	3.75	W
Power Dissipation (QFN32,Ta=70℃) *3	P_{D70}		2.06	
Power Dissipation (QFN32,Ta=85℃) *3	P_{D85}		1.50	
Junction Temperature	T_{jmax}	-	125	ºC
Storage Temperature	T_{STG}	-50	125	ºC
Speaker Impedance	R_{LS}	3.2	-	Ω
Headphone Speaker Impedance	R_{HLS}	12.8	-	Ω

Note) Absolute Maximum Ratings are values which must not be exceeded to guarantee device reliability and life, and when using a device in excess of the ratings for even a moment, it may immediately cause damage to the device or may significantly deteriorate its reliability. In the system where the voltage at an input pin may exceed the supply voltage (V_{AVDD}/GND), use an external diode etc. to limit it to the value lower than absolute maximum rating.

* SPGND=AGND=DGND=CPGND=0V

*1: MIN+, MIN-, LIN1, RIN1, LIN2, and RIN2 pins

*2: θja＝28 ºC /W Condition: Evaluation Board (4 layers), No wind

*3: θja＝27 ºC /W Condition: Evaluation Board (4 layers), No wind

Recommended Operating Conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SPVDD Supply Voltage	V_{SPVDD}	T_A (Min.) = -40 ºC	2.7	3.6	5.25	V
		T_A (Min.) = -30 ºC	2.6			
AVDD Supply Voltage	V_{AVDD}	T_A (Min.) = -40 ºC	2.7	3.0	3.3	V
		T_A (Min.) = -30 ºC	2.6			
HPVDD Supply Voltage	V_{HPVDD}	T_A (Min.) = -40 ºC	2.7	3.0	3.3	V
		T_A (Min.) = -30 ºC	2.6			
Operating Ambient Temperature	T_A		-40	25	85	ºC

* Use the device within the recommended operating conditions.

* SPGND=AGND=DGND=CPGND=0V

* SPVDD ≥ AVDD=HPVDD

* Power up SPVDD and AVDD=HPVDD in this order.

* The slew rate of SPVDD, AVDD, and HPVDD should be less than 1V/µsec.

* When in use, pay attention so that supply voltages do not lower than the shutdown threshold voltage.

Consumption Current

(SPVDD=3.6V, AVDD=HPVDD=3.0V, SPGND=AGND=DGND=CPGND=0V, TA=25ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Speaker Mode						
SPVDD Consumption Current	I_{SPVDD}	No load, No input PD_HP="1"	-	1.5	-	mA
AVDD, HPVDD Consumption Current	I_{VDD}		-	3.5	-	mA
Headphone Mode						
SPVDD Consumption Current	I_{SPVDD}	No load, No input PD_SP="1"	-	1.0	-	µA
AVDD, HPVDD Consumption Current	I_{VDD}		-	8.0	-	mA
Receiver Mode						
SPVDD Consumption Current	I_{SPVDD}	No load, No input PDPC="0", PD_REC="0" Another is Register Default.	-	30	-	µA
AVDD, HPVDD Consumption Current	I_{VDD}		-	1.2	-	mA
Power-down Mode Consumption Current	I_{PD}	Register Default	-	1.0	-	µA

DC Characteristics

(SPVDD=2.7 to 5.25V, AVDD=HPVDD=2.7 to 3.3V, SPGND=AGND=DGND=CPGND=0V, TA=-40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
AVDD Startup Threshold Voltage	V_{UVLH}		-	2.2	-	V
AVDD Shutdown Threshold Voltage	V_{UVLL}		-	2.0	-	V
Digital Input Voltage H Level	V_{IH}	SDA, SCL, /RST	1.4	-	-	V
Digital Input Voltage L Level	V_{IL}	SDA, SCL, /RST	-	-	0.4	V
I^2C Output Voltage	V_{OL}	I_{OL}=3mA SDA	-	-	0.4	V
Input Capacitance	CI	SDA, SCL, /RST	-	-	10	pF
Schmitt Width	V_{sh}	SDA, SCL, /RST	-	200	-	mV
PROTN L Level Output Voltage	$V_{OLPROTN}$	I_{OL}=400µA	-	-	0.4	V
VREF pin Voltage	Vref		-	$V_{AVDD}/2$	-	V

AC Characteristics

(SPVDD=2.7 to 5.25V, AVDD=HPVDD=2.7 to 3.3V, SPGND=AGND=DGND=CPGND=0V, TA=-40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input DC-cut Capacitor Charge Time	T_{CHG}	DC-cut capacitor 0.1µF	-	15	23	msec
Headphone Amplifier Startup Time	T_{STUP2}		-	4	8	msec
Input Resistance	R_{IN}		15	-	180	kΩ
Input Resistance at power down	R_{INPD}	LIN1, RIN1, LIN2, RIN2 pins	-	12	-	kΩ
		MIN+, MIN- pins		6		
Attack Time 0	T_{AT0}	DATT[1:0]=00	-	0.12	-	msec/dB
Attack Time 1	T_{AT1}	DATT[1:0]=01		1.2		
Attack Time 2	T_{AT2}	DATT[1:0]=10		2.4		
Attack Time 3	T_{AT3}	DATT[1:0]=11		5.4		
Release Time 0	T_{RL0}	DREL[1:0]=00	-	0.02	-	sec/dB
Release Time 1	T_{RL1}	DREL[1:0]=01		0.06		
Release Time 2	T_{RL2}	DREL[1:0]=10		0.12		
Release Time 3	T_{RL3}	DREL[1:0]=11		0.30		
Carrier Clock Frequency	F_{PWM}		-	470	-	kHz
PROTN Drive Load Capacitance	C_{PROTN}		-	-	160	pF

Analog Characteristics

Speaker Amplifier

(SPVDD=3.6V, AVDD=HPVDD=3.0V, SPGND=AGND=DGND=CPGND=0V, 1kHz, TA=25ºC, VOL=ATT=0dB, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Output	P_O	SPVDD=5V,R_L=4Ω, THD+N=10%	-	2.6	-	W
		SPVDD=5V,R_L=4Ω,THD+N=1%		2.2		
		R_L=8ΩTHD+N=10%		0.8		
		R_L=8ΩTHD+N=1%		0.68		
Maximum Output in Non-clip control	P_{ONC1}	SPVDD=5V,R_L=4Ω, DALC[2:0]=001	-	1.7	-	W
		R_L=8Ω, DALC[2:0]=001		0.55		
	P_{ONC2}	SPVDD=5V,R_L=4Ω, DALC[2:0]=100	-	2.3	-	W
		R_L=8Ω, DALC[2:0]=100		0.73		
	P_{ONC3}	SPVDD=5V,R_L=4Ω, DALC[2:0]=101	-	2.4	-	W
		R_L=8Ω, DALC[2:0]=101		0.75		
	P_{ONC4}	SPVDD=5V,R_L=4Ω, DALC[2:0]=110	-	2.5	-	W
		R_L=8Ω, DALC[2:0]=110		0.78		
	P_{ONC5}	SPVDD=5V,R_L=4Ω, DALC[2:0]=111	-	2.6	-	W
		R_L=8Ω, DALC[2:0]=111		0.8		
Total Harmonic Distortion (BW:20kHz)	THD+N	R_L=4Ω, P_O=0.65W	-	0.045	-	%
		R_L=8Ω, P_O=0.4W		0.045		
Noise(BW:20kHz A-Filter)	N	MUTE (See Note 2.)	-	40	-	μVrms
S/N Ratio (BW:20kHz A-Filter)	SNR	Monaural differential input	-	90	-	dB
		Stereo input		92		
PSRR	PSRR	217Hz(SPVDD)	-	-75	-	dB
Efficiency	η	R_L=8Ω, P_O=0.8W	-	84	-	%
		R_L=8Ω, P_O=0.1W		75		
Output Offset Voltage	Vo	MUTE (See Note 2.)	-	±20	-	mV
Frequency Characteristics (Cin=0.1uF)	Fres	100Hz to 20kHz	-3	-	4	dB
Non-Clip2 Maximum Attenuation Gain	Aa		-	-8.4	-	dB
Power Limit Output Power (THD+N=10%)	P_{PL1}	R_L=8Ω,DPLT[2:0]=001	-	390	-	mW
	P_{PL2}	R_L=8Ω,DPLT[2:0]=010		470		
	P_{PL3}	R_L=8Ω,DPLT[2:0]=011		600		
	P_{PL4}	R_L=8Ω,DPLT[2:0]=100		780		
	P_{PL5}	R_L=8Ω,DPLT[2:0]=101		900		
	P_{PL6}	R_L=8Ω,DPLT[2:0]=110,SPVDD=4V		1100		

Note1: All analog characteristics were obtained by using our evaluation board. Depending upon pattern layout etc., characteristics may vary. The measurement condition "RL=8Ω" is actually a pure resistor of 8Ω plus 30μH (8Ω+30μH).

Note2: Volume = Mixer = Attenuator = MUTE

Headphone Amplifier

(SPVDD=3.6, AVDD=HPVDD=3.0V, SPGND=AGND=DGND=CPGND=0V, 1kHz, TA=25ºC, VOL=ATT=0dB, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Maximum Output	P_O	WLCSP, R_L=16Ω, THD+N=1%	-	30	-	mW
		QFN, R_L=16Ω, THD+N=1%		27		
Total Harmonic Distortion (BW:20kHz)	THD+N	R_L=16Ω, P_O=5mW	-	0.03	-	%
Noise (BW:20kHz A-Filter)	N	MUTE (See Note2.)	-	10	-	μVrms
S/N Ratio (BW:20kHz A-Filter)	SNR		-	92	-	dB
Output Offset Voltage	Vo	MUTE (See Note2.)	-	±2	-	mV
Frequency Characteristics (Cin=0.1uF)	Fres	100Hz to 20kHz	-3	-	1	dB
Channel Separation	CS	R_L=16Ω	-	90	-	dB

Note1: All analog characteristics were obtained by using our evaluation board. Depending upon pattern layout etc., characteristics may vary.
Note2: Volume =Mixer = Attenuator = MUTE

Receiver Switch

(SPVDD=3.6, AVDD=HPVDD=3.0V, SPGND=AGND=DGND=CPGND=0V, TA=25ºC, unless otherwise specified)

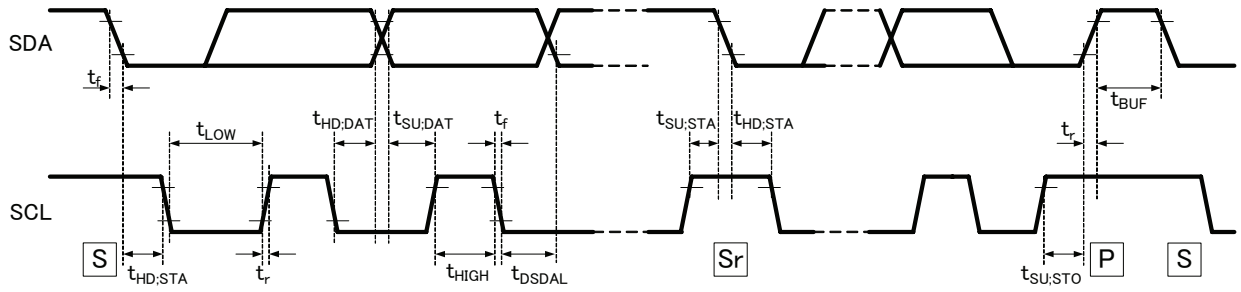
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resistance at Receiver SW ON	Ron		-	1.5	-	Ω

Note1: All analog characteristics were obtained by using our evaluation board. Depending upon pattern layout etc., characteristics may vary.

I²C Timing

(SPVDD=2.7 to 5.25V, AVDD=HPVDD=2.7 to 3.3V, SPGND=AGND=DGND=CPGND=0V, TA=-40ºC to 85ºC, unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Conditions						
SCL Input Clock Frequency	f_{SCL}		0	-	400	kHz
"START" Condition Hold Time	$t_{HD;STA}$		0.6	-	-	ns
SCL Input Clock "L" Time	t_{LOW}		1.3	-	-	ns
SCL Input Clock "H" Time	t_{HIGH}		0.6	-	-	ns
Repeat "START" Condition Setup Time	$t_{SU;STA}$		0.6	-	-	ns
Data Input Hold Time	$t_{HD;DAT}$		0	-	-	ns
Data Input Setup Time	$t_{SU;DAT}$		100	-	-	ns
SDA,SCL Input Rise Time	t_r		-	-	300	ns
SDA,SCL Input Fall Time	t_f		-	-	300	ns
"STOP" Condition Setup Time	$t_{SU;STO}$		0.6	-	-	ns
Bus Free Time between "STOP" and "START" conditions	t_{BUF}		1.3	-	-	ns
Capacitance Load of each bus line	C_b		-	-	400	pF
Output Conditions						
SDA "L" Output Delay Time	t_{DSDAL}		-	-	1.15	µs
Data Output Hold Time	$t_{HD;DAT}$		0	-	0.9	µs

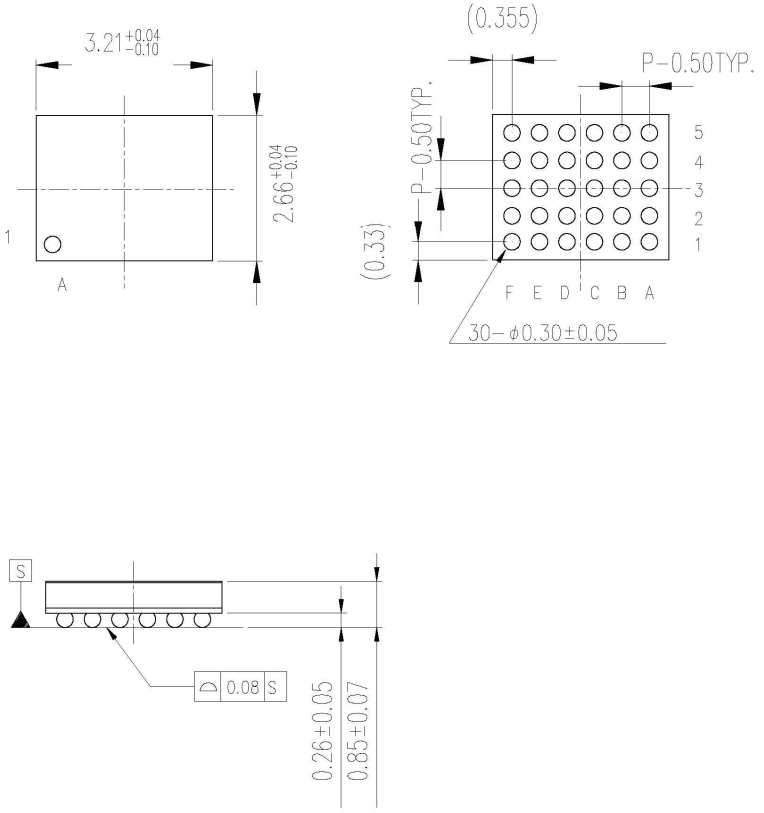


"S": Start Condition, "Sr": Repeatitive Start Condition, "P": Stop Condition

* The measurement was performed at the following conditions:
Input Conditions : V_{IH}=0.8×AVDD, V_{IL}=0.1×AVDD
Measurement Points: V_{OH}=0.7×AVDD, V_{OL}=0.3×AVDD

■ Package Outline (WLCSP)

C-PK30PP-1



カッコ内の寸法値は参考値です。
外形寸法はバリを含みます。
単位： mm

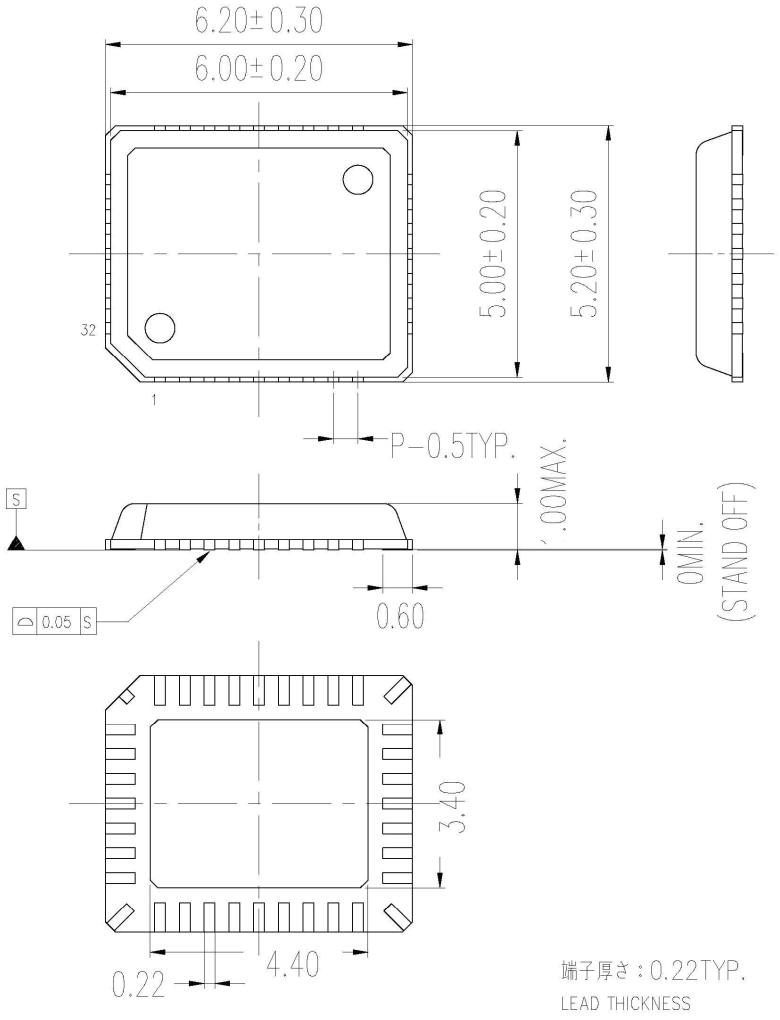
The figure in the parentheses ( ) should be used as a reference.
The dimensions include burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

■ Package Outline (QFN)

C-PK32QP2-2



カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位： mm

The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注） 表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
詳しくはヤマハ代理店までお問い合わせください。

Note: The storage and soldering of LSIs for surface mounting need special consideration.
For detailed information, please contact your local Yamaha agent.

MEMO

IMPORTANT NOTICE

1. YAMAHA RESERVES THE RIGHT TO MAKE CHANGES TO ITS PRODUCTS AND TO THIS DOCUMENT WITHOUT NOTICE. THE INFORMATION CONTAINED IN THIS DOCUMENT HAS BEEN CAREFULLY CHECKED AND IS BELIEVED. HOWEVER, YAMAHA SHALL ASSUME NO RESPONSIBILITIES FOR INACCURACIES AND MAKE NO COMMITMENT TO UPDATE OR TO KEEP CURRENT THE INFORMATION CONTAINED IN THIS DOCUMENT.

2. THESE YAMAHA PRODUCTS ARE DESIGNED ONLY FOR COMMERCIAL AND NORMAL INDUSTRIAL APPLICATIONS, AND ARE NOT SUITABLE FOR OTHER USES, SUCH AS MEDICAL LIFE SUPPORT EQUIPMENT, NUCLEAR FACILITIES, CRITICAL CARE EQUIPMENT OR ANY OTHER APPLICATION THE FAILURE OF WHICH COULD LEAD TO DEATH, PERSONAL INJURY OR ENVIRONMENTAL OR PROPERTY DAMAGE. USE OF THE PRODUCTS IN ANY SUCH APPLICATION IS AT THE CUSTOMER'S OWN RISK AND EXPENSE.

3. YAMAHA SHALL ASSUME NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCT.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANY THIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRINGEMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIFICALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF PRODUCTS. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMES OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

6. YAMAHA MAKES EVERY EFFORT TO IMPROVE THE QUALITY AND RELIABILITY OF ITS PRODUCTS. HOWEVER, ALL SEMICONDUCTOR PRODUCTS FAIL WITH SOME PROBABILITY. THEREFORE, YAMAHA REQUIRES THAT SUFFICIENT CARE BE GIVEN TO ENSURING SAFE DESIGN IN CUSTOMER PRODUCTS SUCH AS REDUNDANT DESIGN, ANTI-CONFLAGRATION DESIGN, AND DESIGN FOR PREVENTING MALFUNCTION IN ORDER TO PREVENT ACCIDENTS RESULTING IN INJURY OR DEATH, FIRE OR OTHER SOCIAL DAMAGE FROM OCCURRING AS A RESULT OF PRODUCT FAILURE.

7. INFORMATION DESCRIBED IN THIS DOCUMENT: APPLICATION CIRCUITS AND ITS CONSTANTS AND CALCULATION FORMULAS, PROGRAMS AND CONTROL PROCEDURES ARE PROVIDED FOR THE PURPOSE OF EXPLAINING TYPICAL OPERATION AND USAGE. THEREFORE, PLEASE EVALUATE THE DESIGN SUFFICIENTLY AS WHOLE SYSTEM UNDER THE CONSIDERATION OF VARIOUS EXTERNAL OR ENVIRONMENTAL CONDITIONS AND DETERMINE THEIR APPLICATION AT THE CUSTOMER'S OWN RISK. YAMAHA SHALL ASSUME NO RESPONSIBILITY FOR CLAIMS, DAMAGES, COSTS AND EXPENSES CAUSED BY THE CUSTOMER OR ANY THIRD PARTY, OWING TO THE USE OF THE ABOVE INFORMATION.

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

YAMAHA CORPORATION

Address inquiries to:
Semiconductor Sales & Marketing Department

■ Head Office 203, Matsunokijima, Iwata,
Shizuoka, 438-0192, Japan
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■ Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568, Japan
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■ Osaka Office 3-12-12, Minami Senba, Chuo-ku,
Osaka City, Osaka, 542-0081, Japan
Tel. +81-6-6252-6221 Fax. +81-6-6252-6229