

**2SA1676,
2SC4396**

T-37-13
T-35-11

2059

PNP/NPN Epitaxial Planar
Silicon Transistors

Switching Applications

(with Bias Resistances $R1=47k\Omega$, $R2=47k\Omega$)

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Applications

- Switching circuit, inverter circuit, interface circuit, driver circuit

Features

- On-chip bias resistance ($R1=47k\Omega$, $R2=47k\Omega$)
- Very small-sized package permitting 2SA1676/2SC4396-applied sets to be made smaller and slimmer

(): 2SA1676

Absolute Maximum Ratings at $T_a=25^\circ\text{C}$

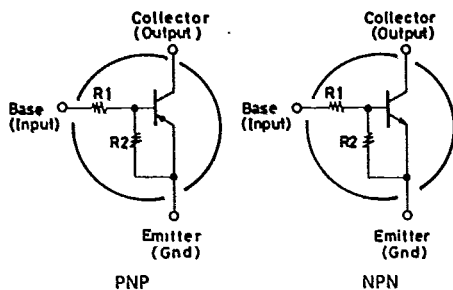
			unit
Collector to Base Voltage	V_{CB0}	(-)50	V
Collector to Emitter Voltage	V_{CE0}	(-)50	V
Emitter to Base Voltage	V_{EB0}	(-)10	V
Collector Current	I_C	(-)100	mA
Peak Collector Current	i_{cp}	(-)200	mA
Collector Dissipation	P_C	150	mW
Junction Temperature	T_j	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Electrical Characteristics at $T_a=25^\circ\text{C}$

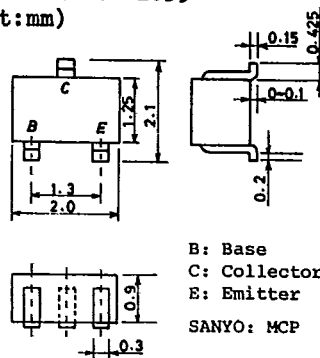
			min	typ	max	unit
Collector Cutoff Current	I_{CB0}	$V_{CB}=(-)40\text{V}, I_E=0$			(-)0.1	μA
Collector Cutoff Current	I_{CE0}	$V_{CE}=(-)40\text{V}, I_B=0$			(-)0.5	μA
Emitter Cutoff Current	I_{EB0}	$V_{EB}=(-)5\text{V}, I_C=0$	(-)30	(-)53	(-)80	μA
DC Current Gain	h_{FE}	$V_{CE}=(-)5\text{V}, I_C=(-)5\text{mA}$	50			
Gain-Bandwidth Product	f_T	$V_{CE}=(-)10\text{V}, I_C=(-)5\text{mA}$		250		MHz
				(200)		MHz
Output Capacitance	c_{ob}	$V_{CB}=(-)10\text{V}, f=1\text{MHz}$		3.3		pF
				(5.1)		pF
C-E Saturation Voltage	$V_{CE(sat)}$	$I_C=(-)5\text{mA}, I_B=(-)0.25\text{mA}$		(-)0.1	(-)0.3	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	$I_C=(-)10\mu\text{A}, I_E=0$	(-)50			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	$I_C=(-)100\mu\text{A}, R_{BE}=\infty$	(-)50			V
Input OFF-State Voltage	$V_{I(off)}$	$V_{CE}=(-)5\text{V}, I_C=(-)100\mu\text{A}$	(-)0.8	(-)1.1	(-)1.5	V
Input ON-State Voltage	$V_{I(on)}$	$V_{CE}=(-)0.2\text{V}, I_C=(-)5\text{mA}$	(-)1.0	(-)2.5	(-)5.0	V
Input Resistance	R1		32	47	62	kohm
Resistance Ratio	R1/R2		0.9	1.0	1.1	

Marking 2SA1676:BL, 2SC4396:BY

Electrical Connection



Case Outline 2059
(unit:mm)



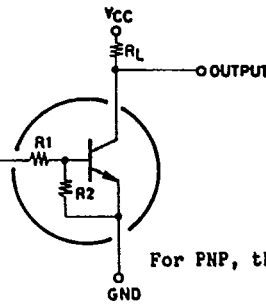
Sample Application Circuit

Input ON-State voltage: 5V or more

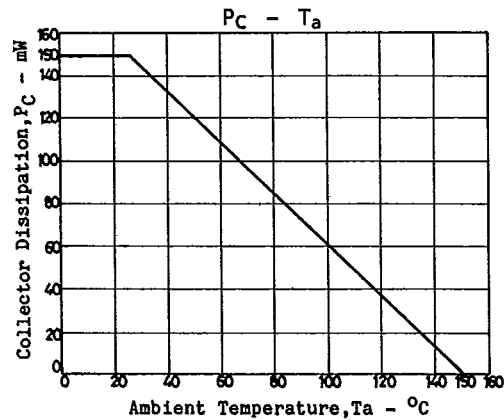
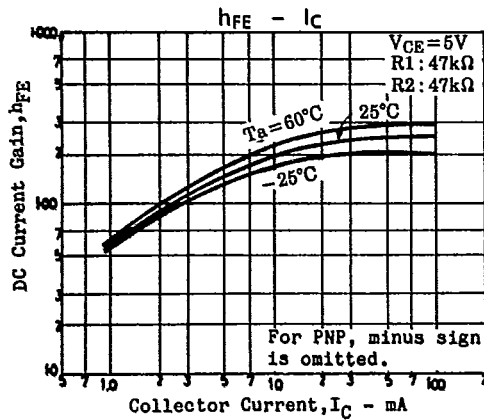
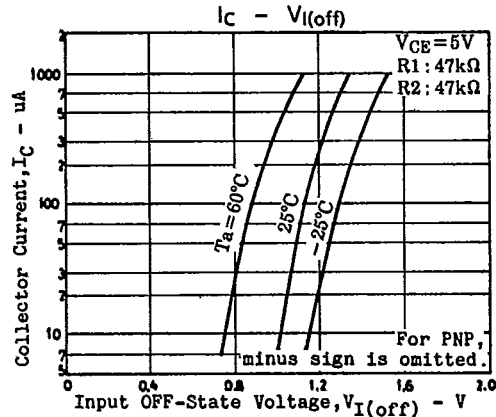
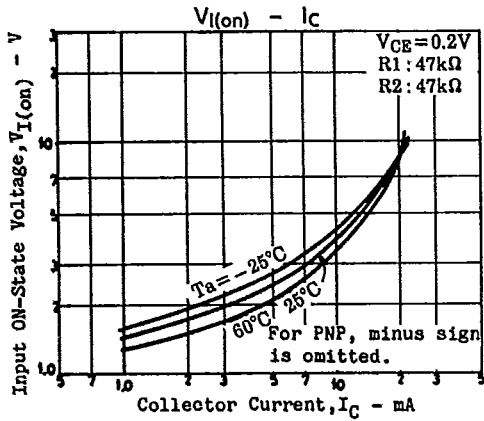
Input OFF-State voltage: 0.8V or less



INPUT



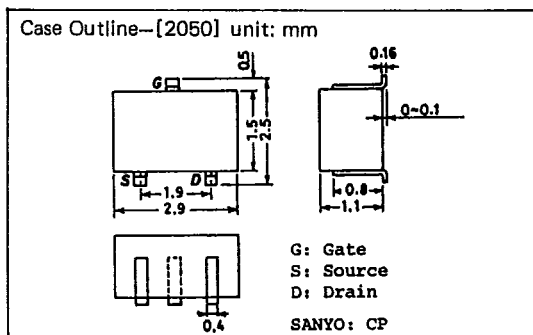
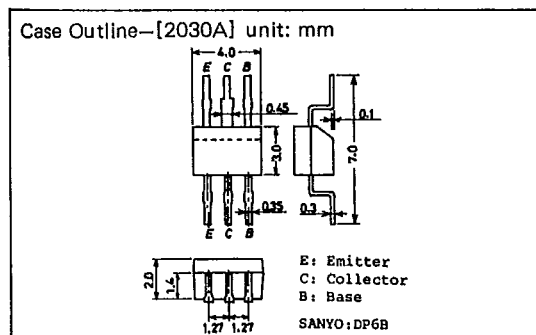
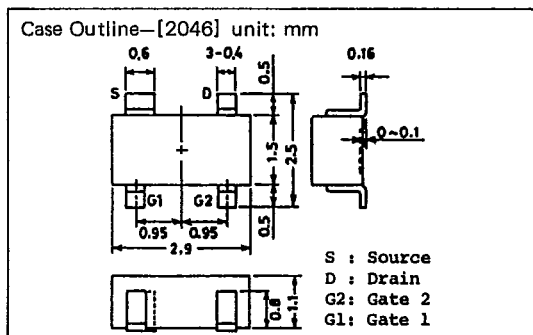
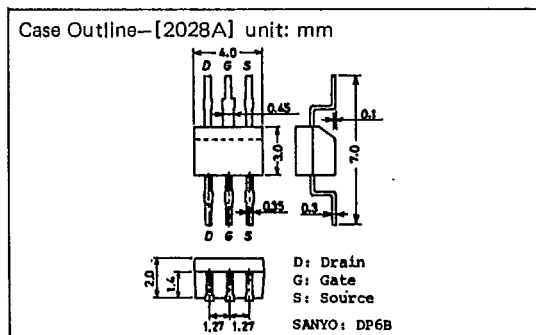
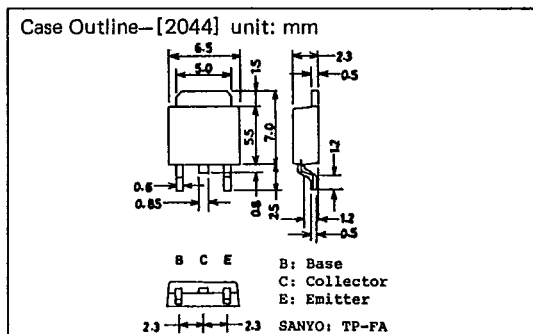
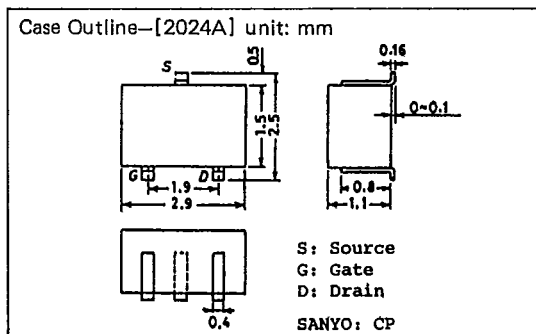
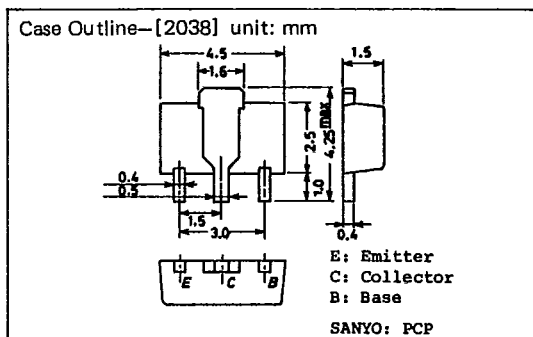
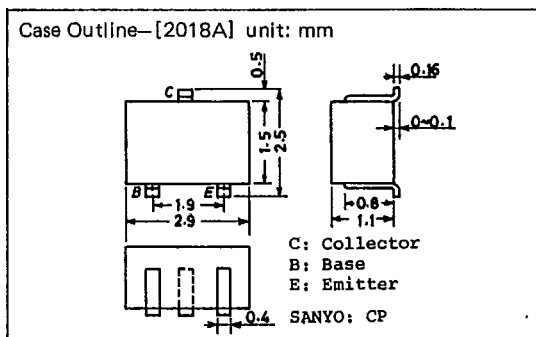
For PNP, the polarity is reversed.



T-91-20

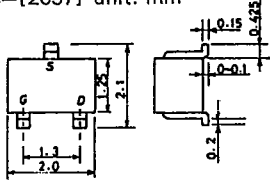
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



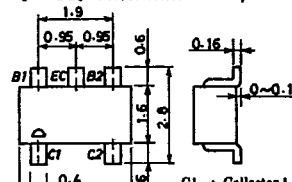
T-91-20

Case Outline—[2057] unit: mm



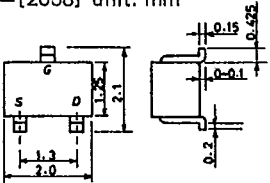
S: Source
G: Gate
D: Drain
SANYO: MCP

Case Outline—[2066] unit: mm



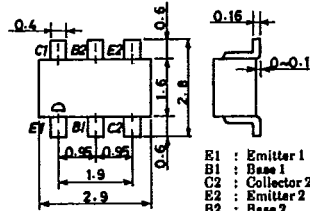
C1 : Collector 1
C2 : Collector 2
B2 : Base 2
EC : Emitter Common
B1 : Base 1
SANYO : CP6

Case Outline—[2058] unit: mm



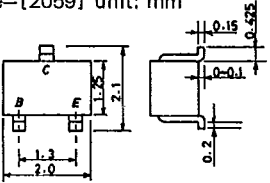
G: Gate
S: Source
D: Drain
SANYO: MCP

Case Outline—[2067] unit: mm



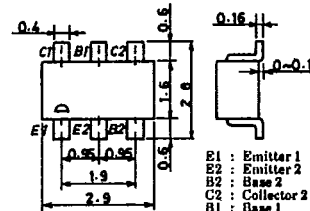
E1 : Emitter 1
B1 : Base 1
C2 : Collector 2
E2 : Emitter 2
B2 : Base 2
C1 : Collector 1
SANYO : CP6

Case Outline—[2059] unit: mm



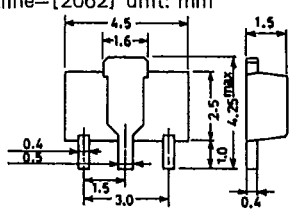
B: Base
C: Collector
E: Emitter
SANYO: MCP

Case Outline—[2068] unit: mm



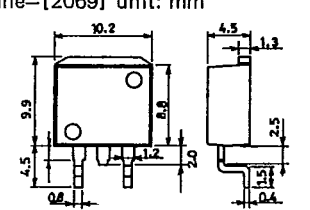
B1 : Emitter 1
E2 : Emitter 2
B2 : Base 2
C2 : Collector 2
B1 : Base 1
C1 : Collector 1
SANYO : CP6

Case Outline—[2062] unit: mm



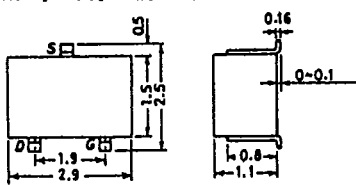
S: Source
D: Drain
G: Gate
SANYO: PCP

Case Outline—[2069] unit: mm



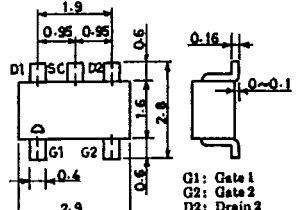
B: Base
C: Collector
E: Emitter
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source
D: Drain
G: Gate
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1
G2 : Gate 2
D2 : Drain 2
SC : Source Common
D1 : Drain 1
SANYO : CP6

T-9120

