June 2000 PRELIMINARY

FDC604P

FAIRCHILD

P-Channel 1.8V Specified PowerTrench[®] MOSFET

General Description

This P-Channel 1.8V specified MOSFET uses Fairchild's low voltage PowerTrench process. It has been optimized for battery power management applications.

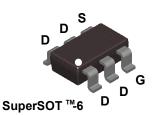
Applications

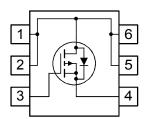
- Battery management
- Load switch
- Battery protection

Features

• -5.5 A, -20 V. $R_{DS(ON)} = 0.033 \Omega \textcircled{O} V_{GS} = -4.5 V$ $R_{DS(ON)} = 0.043 \Omega \textcircled{O} V_{GS} = -2.5 V$ $R_{DS(ON)} = 0.060 \Omega \textcircled{O} V_{GS} = -1.8 V$

- Fast switching speed.
- High performance trench technology for extremely low $R_{\text{DS}(\text{ON})}$





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		-20	V
V _{GSS}	Gate-Source Voltage		±8	V
ID	Drain Current – Continuous	(Note 1a)	-5.5	A
	– Pulsed		-20	
PD	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.604	FDC604P	7"	8mm	3000 units

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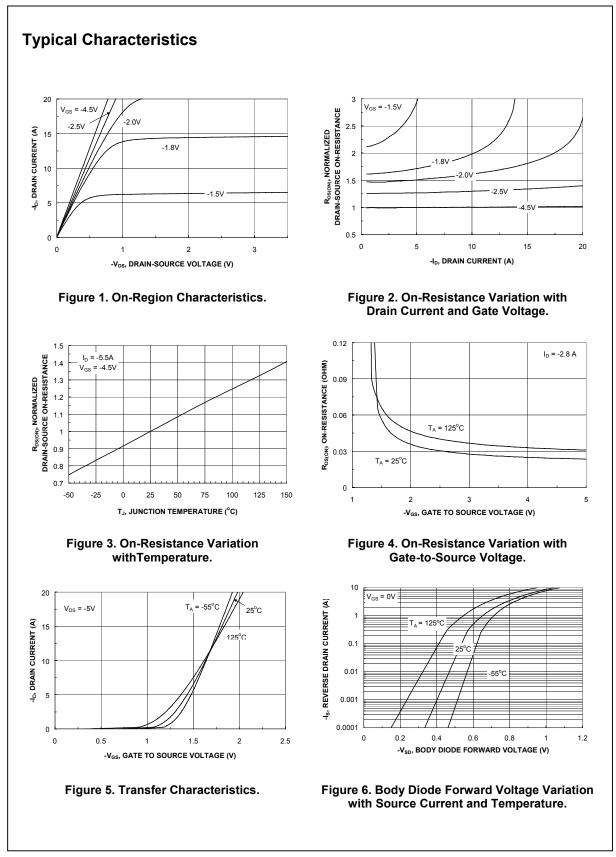
Symbol	Parameter	Test Conditions	Min	Тур	Мах	Units
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_{D} = -250 μ A	-20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA,Referenced to 25°C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 V$, $V_{GS} = 0 V$			-1	μA
GSSF	Gate–Body Leakage, Forward	$V_{GS} = 8 V$, $V_{DS} = 0 V$			100	nA
GSSR	Gate–Body Leakage, Reverse	$V_{GS} = -8 V$ $V_{DS} = 0 V$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	-0.4	-0.7	-1.5	V
<u>ΔV_{GS(th)}</u> ΔT _J	Gate Threshold Voltage Temperature Coefficient	I_D = -250 µA,Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{ll} V_{GS} = -4.5 \ V, & I_D = -5.5 \ A \\ V_{GS} = -2.5 \ V, & I_D = -4.8 \ A \\ V_{GS} = -1.8 \ V, & I_D = -4.0 \ A \end{array} $		0.024 0.030 0.042	0.033 0.043 0.060	Ω
I _{D(on)}	On–State Drain Current	$V_{GS} = -4.5 V$, $V_{DS} = -5 V$	-20			А
g fs	Forward Transconductance	$V_{DS} = -5 V$, $I_{D} = -3.5 A$		23		S
Dynamic	c Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = -10 V$, $V_{GS} = 0 V$,		1926		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		530		pF
C _{rss}	Reverse Transfer Capacitance			185		pF
Switchir	ng Characteristics (Note 2)					
t _{d(on)}	Turn–On Delay Time	$V_{DD} = -10 V$, $I_D = -1 A$,		13	23	ns
tr	Turn–On Rise Time	V_{GS} = -4.5 V, R_{GEN} = 6 Ω		11	20	ns
t _{d(off)}	Turn–Off Delay Time	7		90	144	ns
t _f	Turn–Off Fall Time	7		45	72	ns
Qg	Total Gate Charge	$V_{DS} = -10 V$, $I_{D} = -3.5 A$,		19	30	nC
Q _{gs}	Gate-Source Charge	$V_{GS} = -4.5 V$		4		nC
Q _{gd}	Gate–Drain Charge			7.5		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				-1.3	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 V$, $I_S = -1.3 A$ (Note 2)		-0.7	-1.2	V

 R_{0JA} is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.

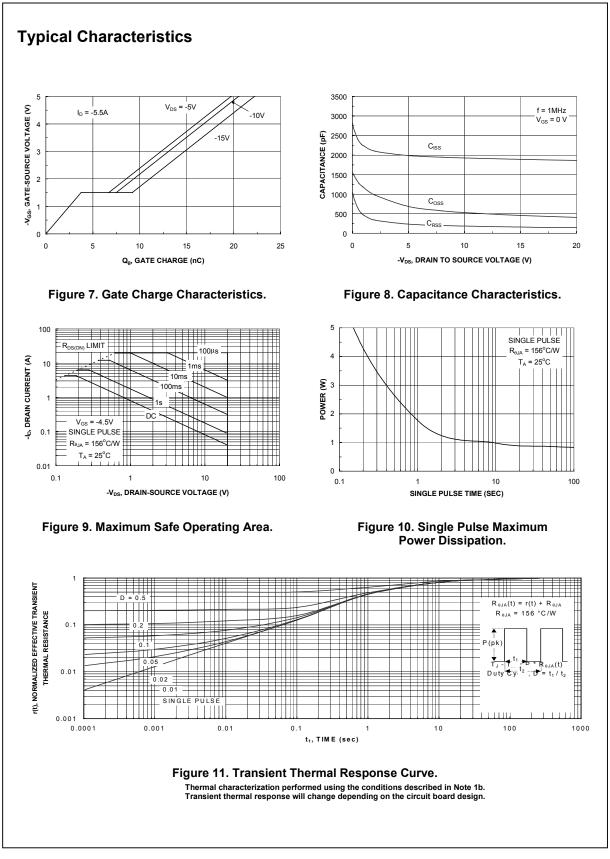
a. 78°C/W when mounted on a $1in^2$ pad of 2oz copper on FR-4 board.

b. 156°C/W when mounted on a minimum pad.

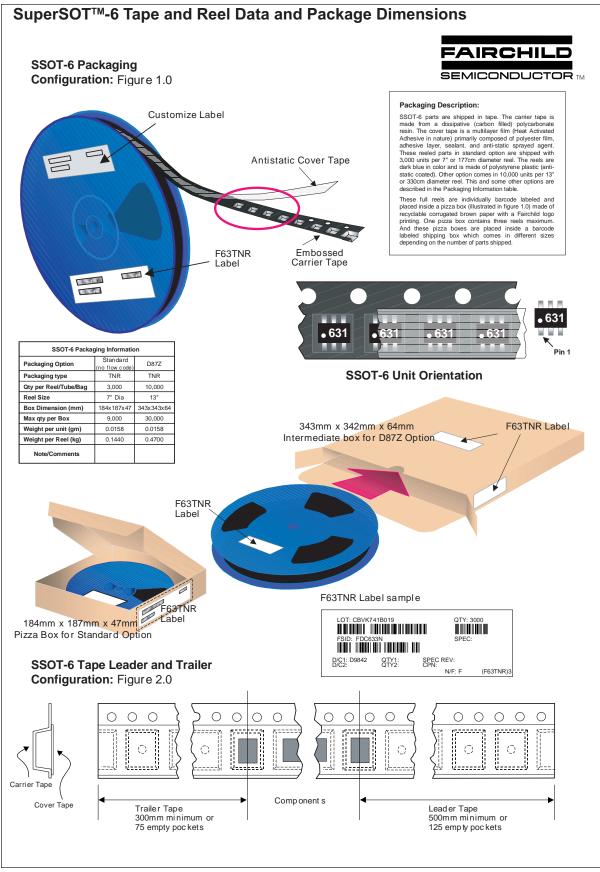
2. Pulse Test: Pulse Width \leq 300 $\mu s,$ Duty Cycle \leq 2.0%



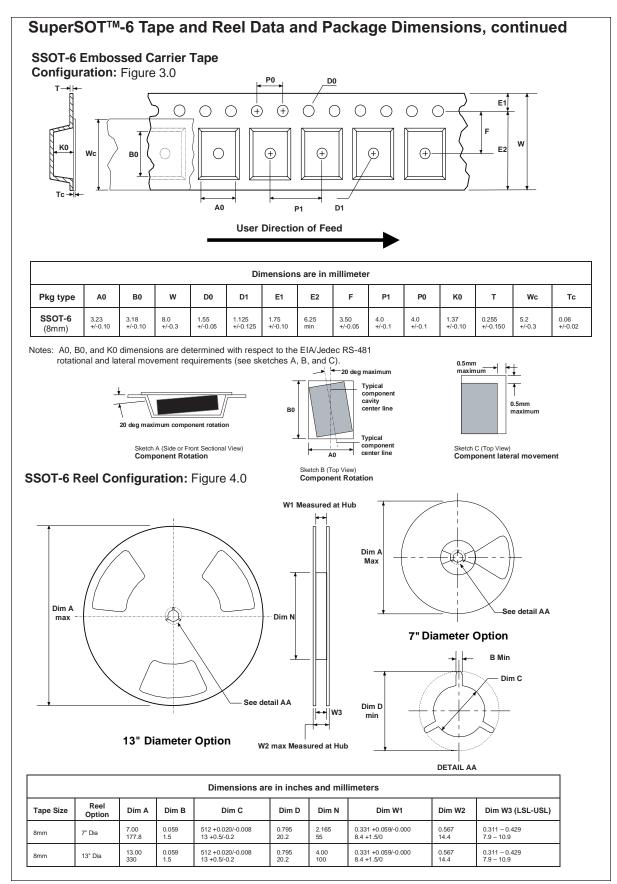
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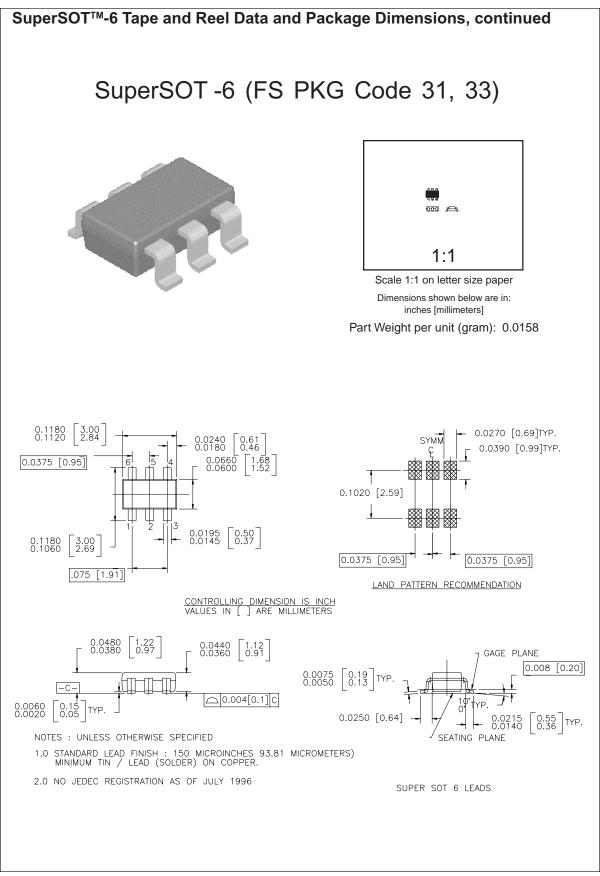
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August 1999, Rev. C



July 1999, Rev. C



September 1998, Rev. A

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