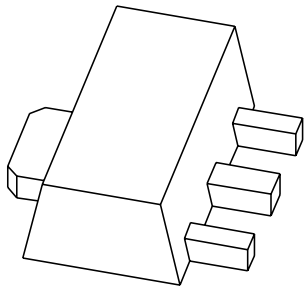


# DATA SHEET



## **PXT2222A** NPN switching transistor

Product specification  
Supersedes data of 1997 May 05

1999 Apr 14

# NPN switching transistor

# PXT2222A

### FEATURES

- High current (max. 600 mA)
- Low voltage (max. 40 V).

### APPLICATIONS

- General purpose switching and linear amplification.

### DESCRIPTION

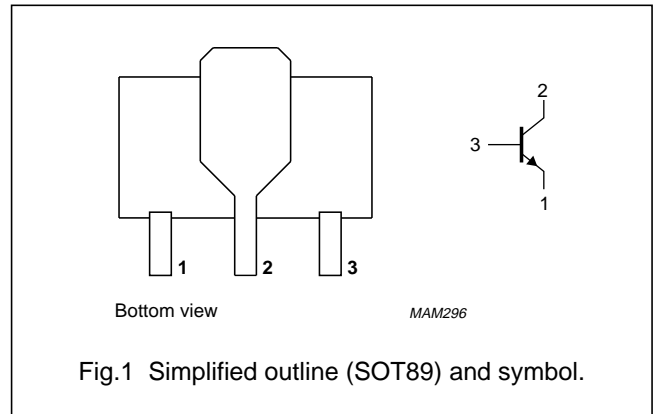
NPN switching transistor in a SOT89 plastic package.  
PNP complement: PXT2907A.

### MARKING

TYPE NUMBER	MARKING CODE
PXT2222A	p1P

### PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	75	V
$V_{CEO}$	collector-emitter voltage	open base	–	40	V
$V_{EBO}$	emitter-base voltage	open collector	–	6	V
$I_C$	collector current (DC)		–	600	mA
$I_{CM}$	peak collector current		–	800	mA
$I_{BM}$	peak base current		–	200	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.25	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

### Note

1. Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 6 cm<sup>2</sup>.  
For other mounting conditions, see “Thermal considerations for SOT89 in the General Part of associated Handbook”.

## NPN switching transistor

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## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	100	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		20	K/W

## Note

- Device mounted on a printed-circuit board, single-sided copper, tinplated, mounting pad for collector 6 cm<sup>2</sup>.  
For other mounting conditions, see "Thermal considerations for SOT89 in the General Part of associated Handbook".

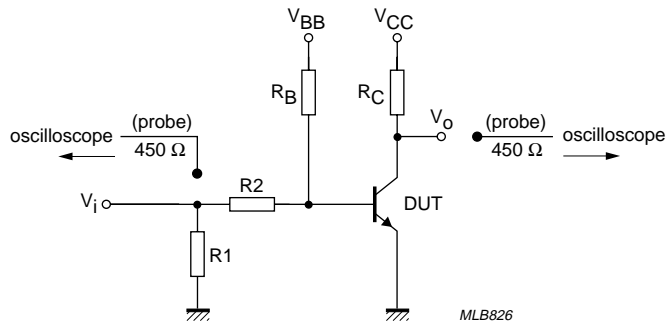
## CHARACTERISTICS

$T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = 60\text{ V}$	–	10	nA
		$I_E = 0; V_{CB} = 60\text{ V}; T_{amb} = 125\text{ °C}$	–	10	μA
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{BE} = 5\text{ V}$	–	10	nA
$h_{FE}$	DC current gain	$I_C = 0.1\text{ mA}; V_{CE} = 10\text{ V}$	35	–	
		$I_C = 1\text{ mA}; V_{CE} = 10\text{ V}$	50	–	
		$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	75	–	
		$I_C = 10\text{ mA}; V_C = 10\text{ V}; T_{amb} = -55\text{ °C}$	35	–	
		$I_C = 150\text{ mA}; V_{CE} = 1\text{ V}$	50	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	100	300	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 150\text{ mA}; I_B = 15\text{ mA}$	–	300	mV
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	1	V
$V_{BEsat}$	base-emitter saturation voltage	$I_C = 150\text{ mA}; I_B = 15\text{ mA}$	0.6	1.2	V
		$I_C = 500\text{ mA}; I_B = 50\text{ mA}$	–	2	V
$C_c$	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	–	8	pF
$C_e$	emitter capacitance	$I_C = i_c = 0; V_{EB} = 500\text{ mV}; f = 1\text{ MHz}$	–	25	pF
$f_T$	transition frequency	$I_C = 20\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	300	–	MHz
F	noise figure	$I_C = 200\text{ μA}; V_{CE} = 5\text{ V}; R_S = 2\text{ k}\Omega;$ $f = 1\text{ kHz}; B = 200\text{ Hz}$	–	4	dB
<b>Switching times (between 10% and 90% levels); (see Fig.2)</b>					
$t_{on}$	turn-on time	$I_{Con} = 150\text{ mA}; I_{Bon} = 15\text{ mA};$ $I_{Boff} = -15\text{ mA}$	–	35	ns
$t_d$	delay time		–	15	ns
$t_r$	rise time		–	20	ns
$t_{off}$	turn-off time		–	250	ns
$t_s$	storage time		–	200	ns
$t_f$	fall time		–	60	ns

NPN switching transistor

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$V_i = 9.5 \text{ V}$ ;  $T = 500 \text{ } \mu\text{s}$ ;  $t_p = 10 \text{ } \mu\text{s}$ ;  $t_r = t_f \leq 3 \text{ ns}$ .  
 $R_1 = 68 \text{ } \Omega$ ;  $R_2 = 325 \text{ } \Omega$ ;  $R_B = 325 \text{ } \Omega$ ;  $R_C = 160 \text{ } \Omega$ .  
 $V_{BB} = -3.5 \text{ V}$ ;  $V_{CC} = 29.5 \text{ V}$ .  
 Oscilloscope: input impedance  $Z_i = 50 \text{ } \Omega$ .

Fig.2 Test circuit for switching times.

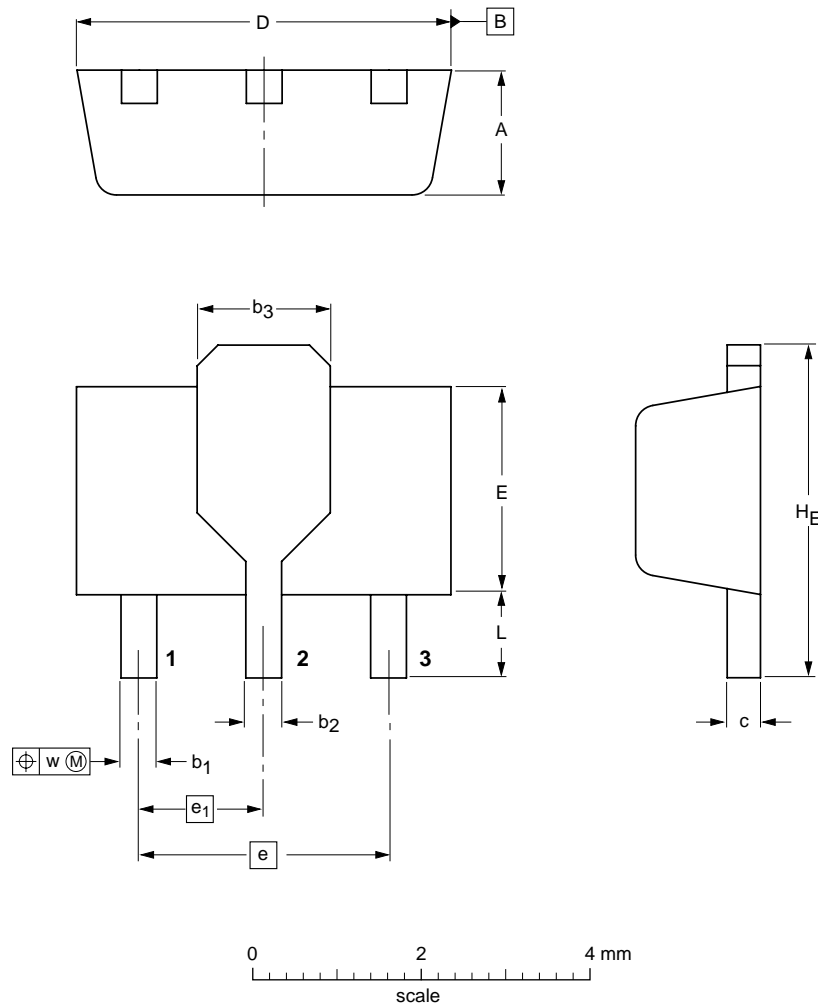
NPN switching transistor

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b <sub>1</sub>	b <sub>2</sub>	b <sub>3</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

## NPN switching transistor

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
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NPN switching transistor

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