
2SJ244

Silicon P-Channel MOS FET

HITACHI

Application

High speed power switching

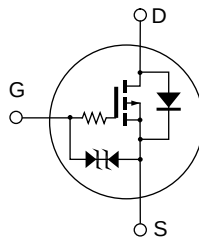
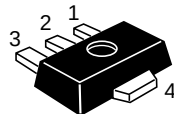
Low voltage operation

Features

- Very Low on-resistance
- High speed switching
- Suitable for camera or VTR motor drive circuit, power switch, solenoid drive and etc.

Outline

UPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-12	V
Gate to source voltage	V_{GSS}	± 7	V
Drain current	I_D	± 2	A
Drain peak current	$I_{D(pulse)}^{*1}$	± 4	A
Channel dissipation	P_{ch}^{*2}	1	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

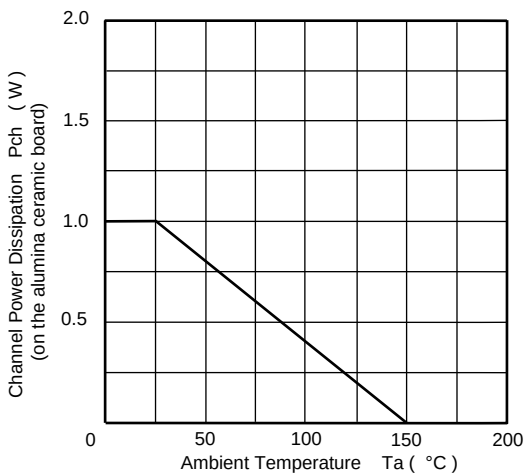
Notes: 1. $PW \leq 100 \mu s$, duty cycle $\leq 10\%$
2. Value on the alumina ceramic board (12.5×20×0.7 mm)
3. Marking is “JY”.

Electrical Characteristics (Ta = 25°C)

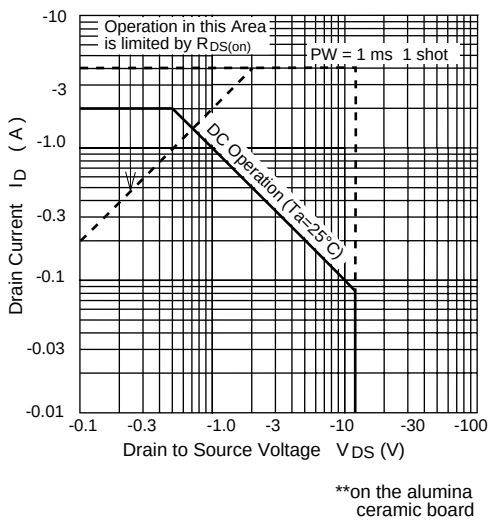
Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-12	—	—	V	$I_D = -1 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 7	—	—	V	$I_G = \pm 10 \mu A$, $V_{DS} = 0$
Gate to source cutoff current	I_{GSS}	—	—	± 5	μA	$V_{GS} = \pm 6 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -8 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.4	—	-1.4	V	$I_D = -100 \mu A$, $V_{DS} = -5 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)1}$	—	0.65	0.9	Ω	$I_D = -0.5 \text{ A}^{*1}$, $V_{GS} = -2.5 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)2}$	—	0.5	—	Ω	$I_D = -1 \text{ A}^{*1}$, $V_{GS} = -4 \text{ V}$
Forward transfer admittance	$ y_{fs} $	—	1.8	—	S	$I_D = -1 \text{ A}^{*1}$, $V_{DS} = -5 \text{ V}$
Input capacitance	C_{iss}	—	130	—	pF	$V_{DS} = -5 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	50	—	pF	
Reverse transfer capacitance	C_{rss}	—	260	—	pF	
Turn-on delay time	$t_{(on)}$	—	365	—	ns	$I_D = -0.2 \text{ A}^{*1}$, $V_{in} = -4 \text{ V}$,
Turn-off delay time	$t_{(off)}$	—	1450	—	ns	$R_L = 51 \Omega$
Body to drain diode forward voltage	V_{DF}	—	—	7	V	$I_F = 4 \text{ A}^{*1}$, $V_{GS} = 0$

Note: 1. Pulse test

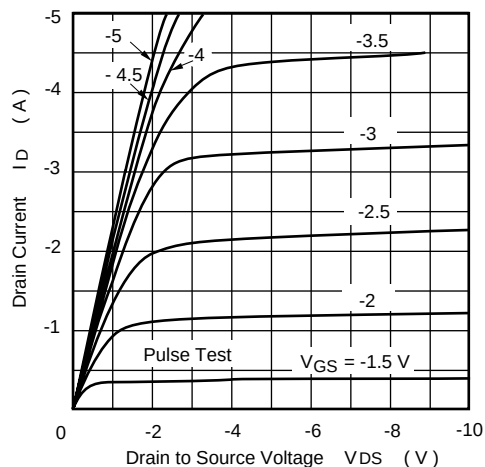
Maximum Channel Power Dissipation Curve



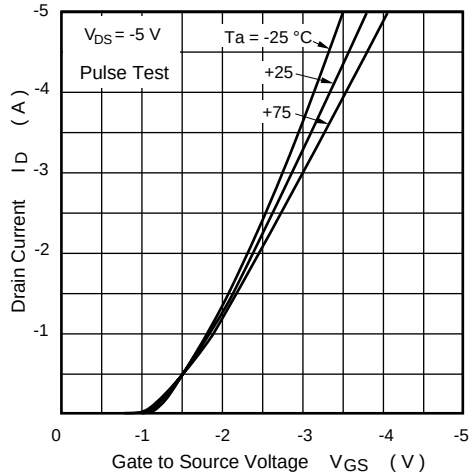
Maximum Safe Operation Area



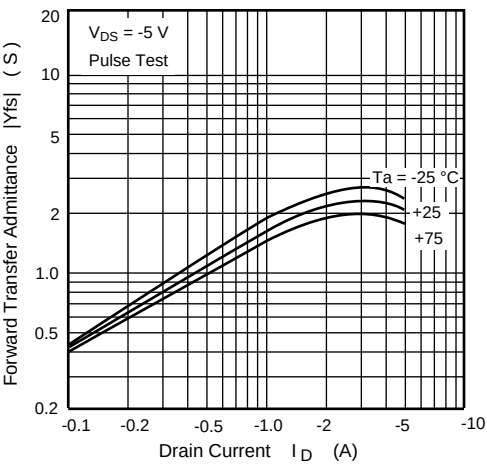
Typical Output Characteristics



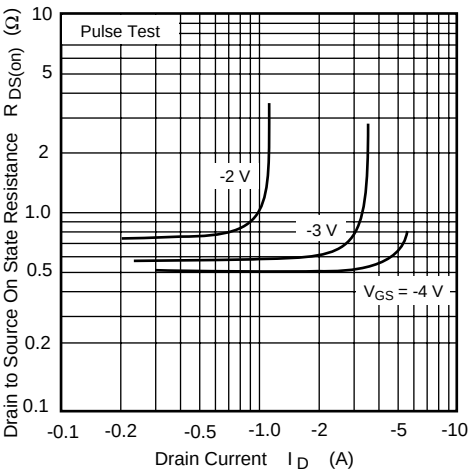
Typical Forward Transfer Characteristics



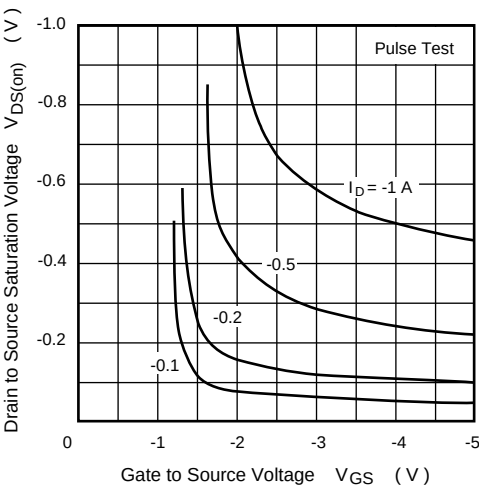
Forward Transfer Admittance vs.
Drain Current



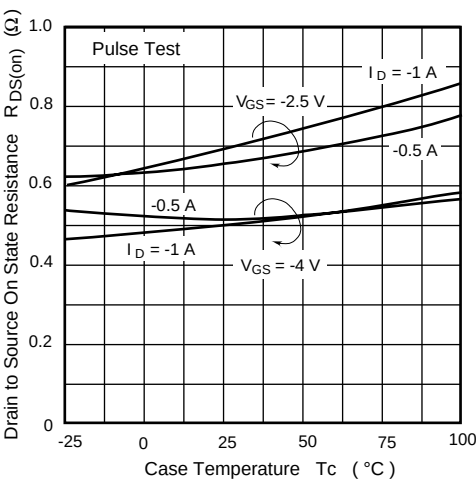
Drain to Source on State Resistance vs.
Drain Current



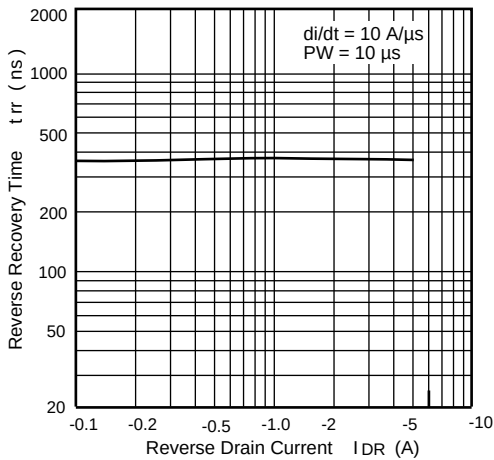
Drain to Source Saturation Voltage vs.
Gate to Source Voltage



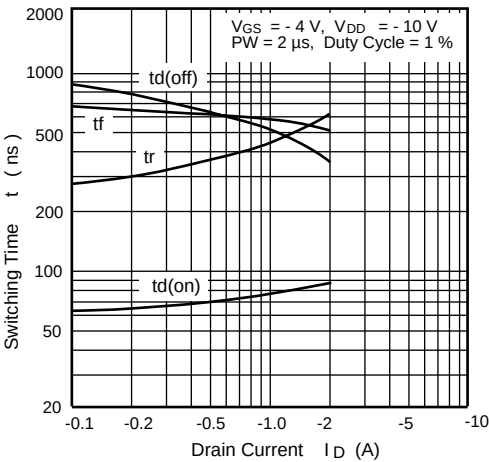
Drain to Source on State Resistance vs.
Case Temperature



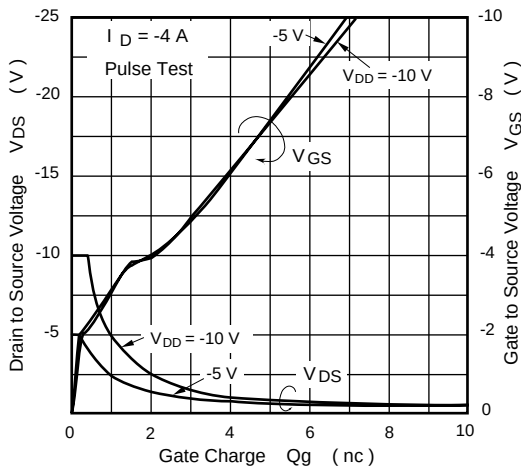
Reverse Recovery Time vs.
Reverse Drain Current



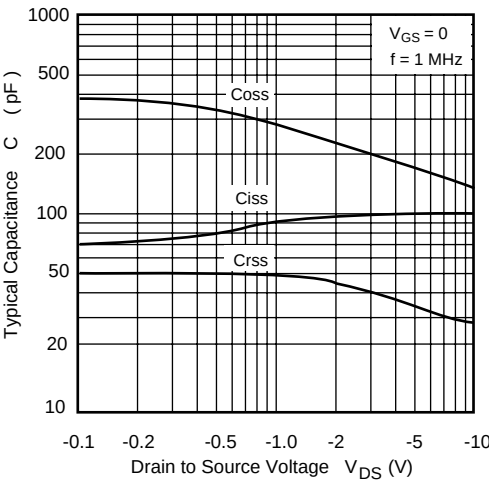
Switching Time vs. Drain Current



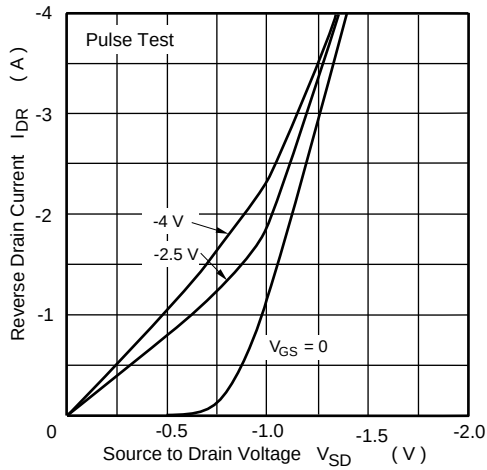
Dynamic Input Characteristics

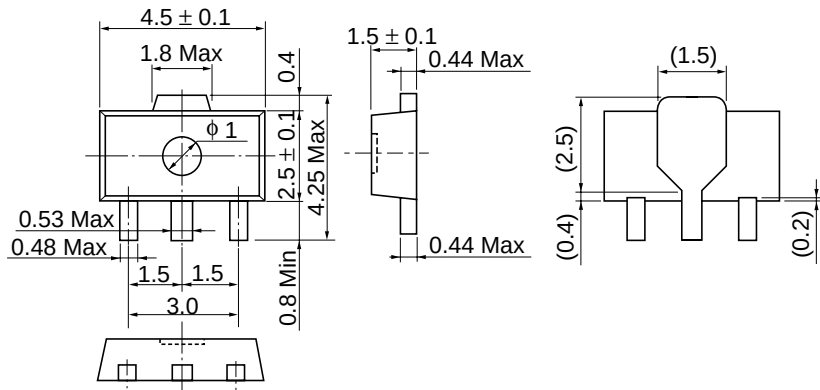


Typical Capacitance vs.
Drain to Source Voltage



Reverse Drain Current vs.
Source to Drain Voltage





Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.050 g

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