

2SJ518

Silicon P Channel MOS FET
High Speed Power Switching

HITACHI

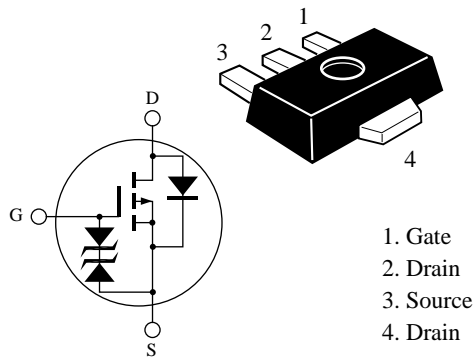
ADE-208-580B (Z)
3rd. Edition
Jul. 1998

Features

- Low on-resistance
 $R_{DS(on)} = 0.35 \Omega$ typ. at ($V_{GS} = -10V, I_D = -1A$)
- Low drive current
- 4 V gate drive devices
- High speed switching

Outline

UPAK



Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_{D}	-2	A
Drain peak current	$I_{\text{D(pulse)}}^{\text{Note1}}$	-4	A
Body-drain diode reverse drain current	I_{DR}	-2	A
Avalanche current	$I_{\text{AP}}^{\text{Note2}}$	-2	A
Avalanche energy	E_{AR}	0.34	mJ
Channel dissipation	$P_{\text{ch}}^{\text{Note3}}$	1	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Note:
1. $PW \leq 10\mu\text{s}$, duty cycle $\leq 1\%$
 2. value at $T_{\text{ch}} = 25^\circ\text{C}$, $R_g \geq 50\ \Omega$
 3. Value at when using the aluminaceramic board (12.5x20x0.7mm)

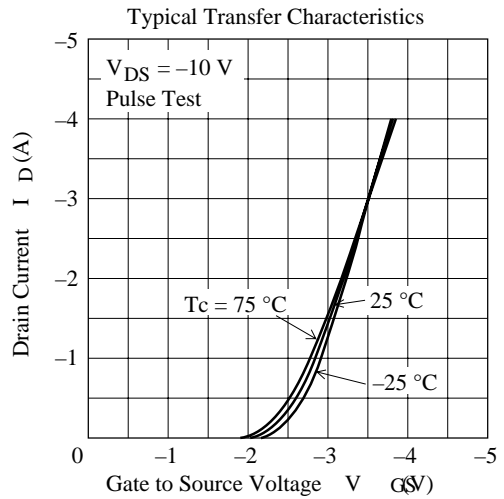
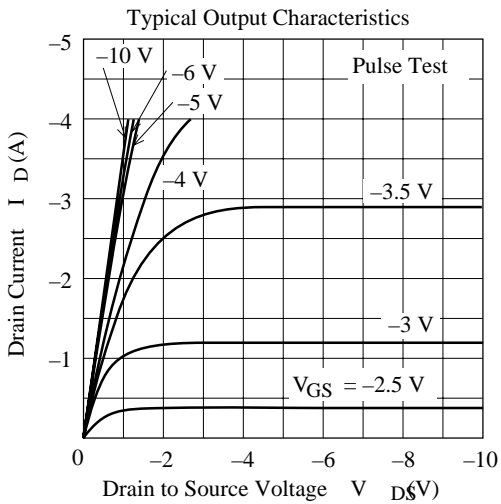
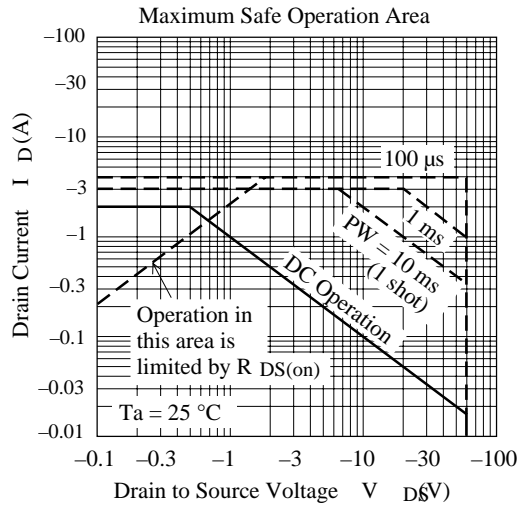
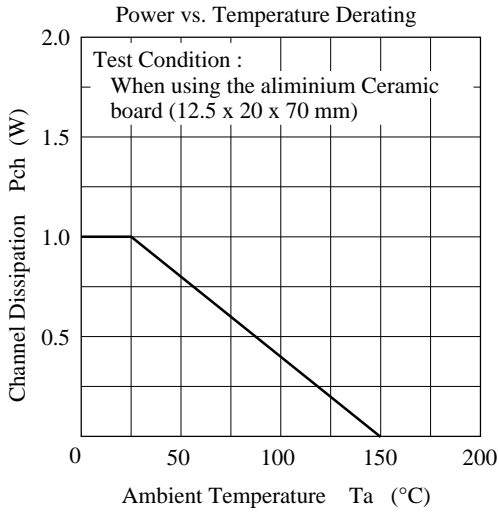
Electrical Characteristics (Ta = 25°C)

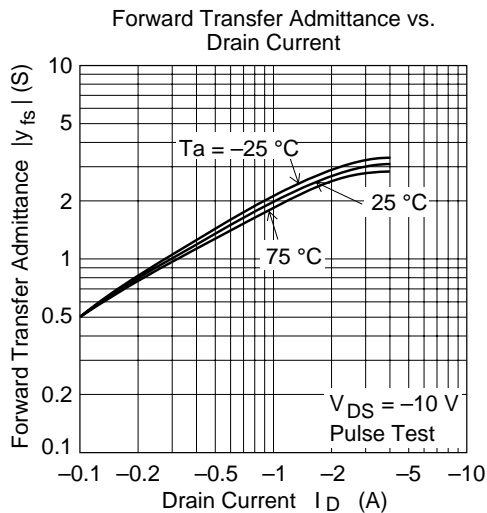
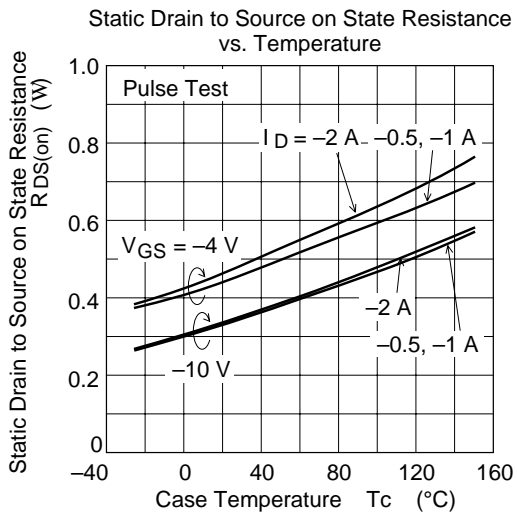
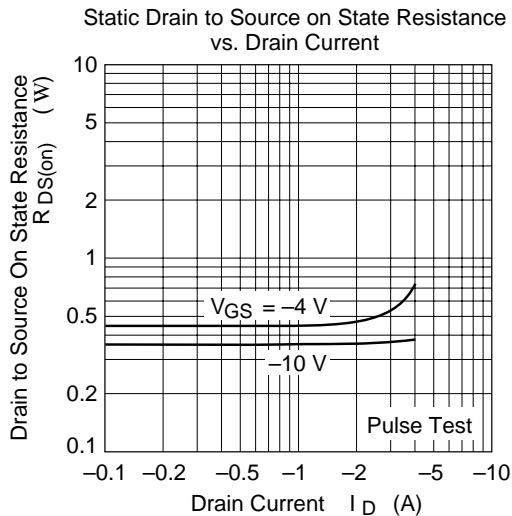
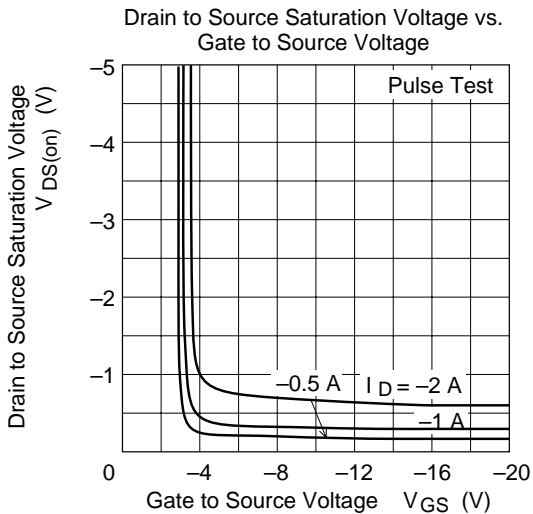
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.0	V	$I_D = -1\text{mA}$, $V_{DS} = -10\text{V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.35	0.46	Ω	$I_D = -1\text{A}$, $V_{GS} = -10\text{V}$ ^{Note4}
	$R_{DS(on)}$	—	0.45	0.63	Ω	$I_D = -1\text{A}$, $V_{GS} = -4\text{V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	1.2	2.0	—	S	$I_D = -1\text{A}$, $V_{DS} = -10\text{V}$ ^{Note4}
Input capacitance	C_{iss}	—	220	—	pF	$V_{DS} = -10\text{V}$
Output capacitance	C_{oss}	—	110	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	35	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	10	—	ns	$V_{GS} = -10\text{V}$, $I_D = -1\text{A}$
Rise time	t_r	—	11	—	ns	$R_L = 30\Omega$
Turn-off delay time	$t_{d(off)}$	—	45	—	ns	
Fall time	t_f	—	30	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-1.05	—	V	$I_D = -2\text{A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = -2\text{A}$, $V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

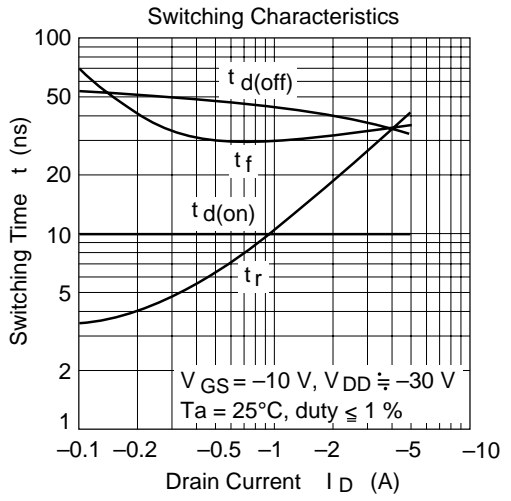
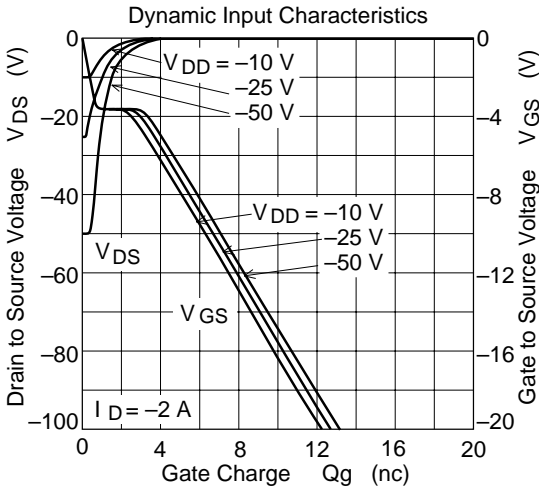
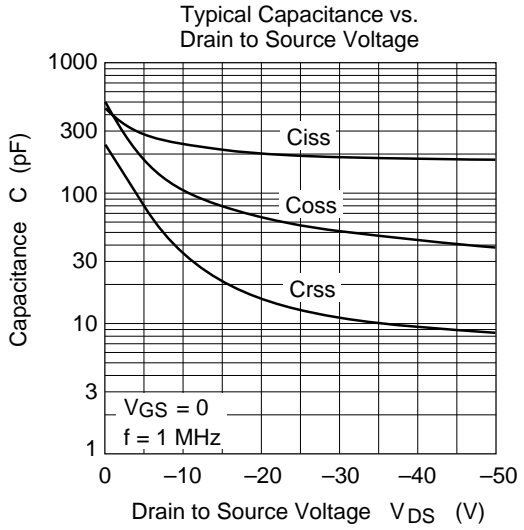
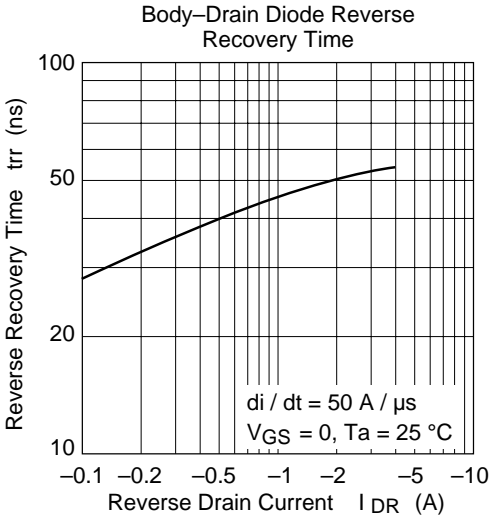
Note: 4. Pulse test

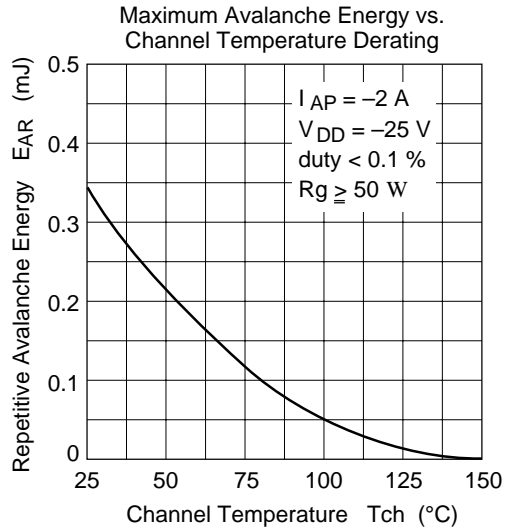
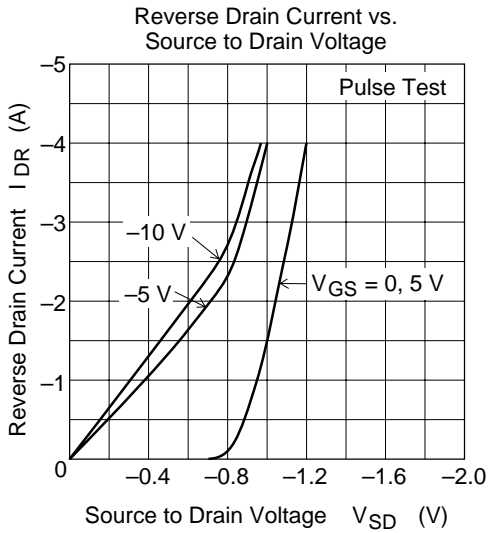
5. Marking is "AZ"

Main Characteristics

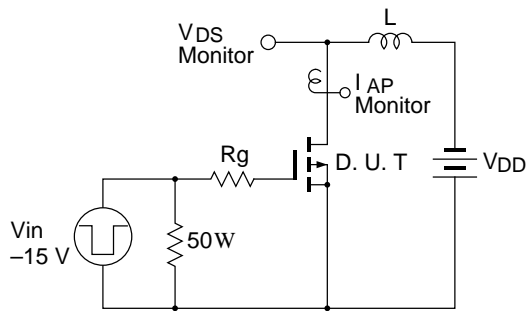






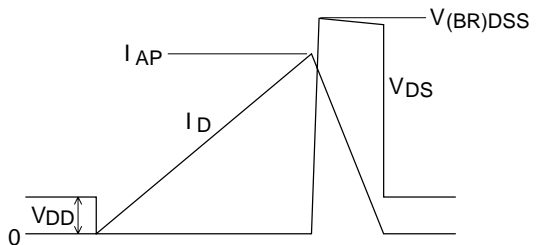


Avalanche Test Circuit

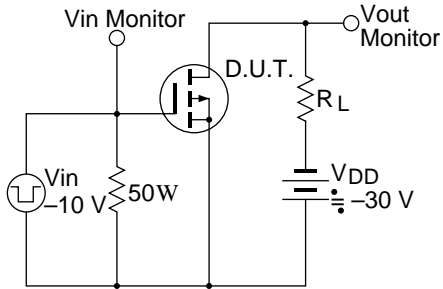


Avalanche Waveform

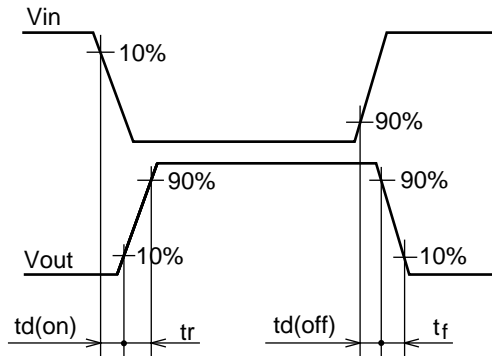
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

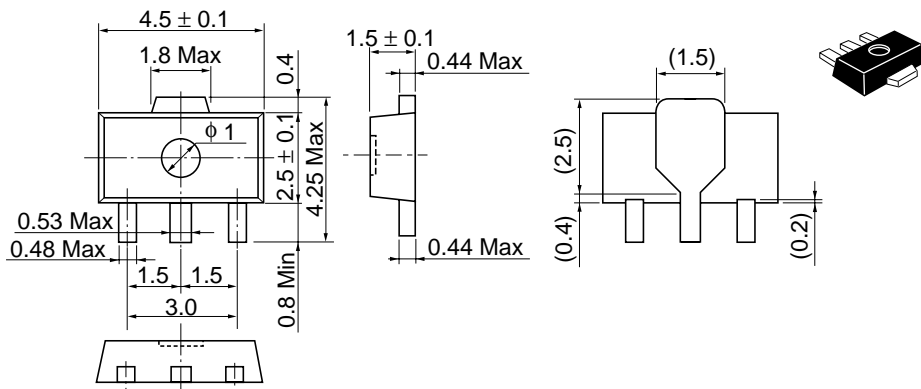


Waveform



Package Dimensions

As of January, 2001
Unit: mm



Hitachi Code	UPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.050 g

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