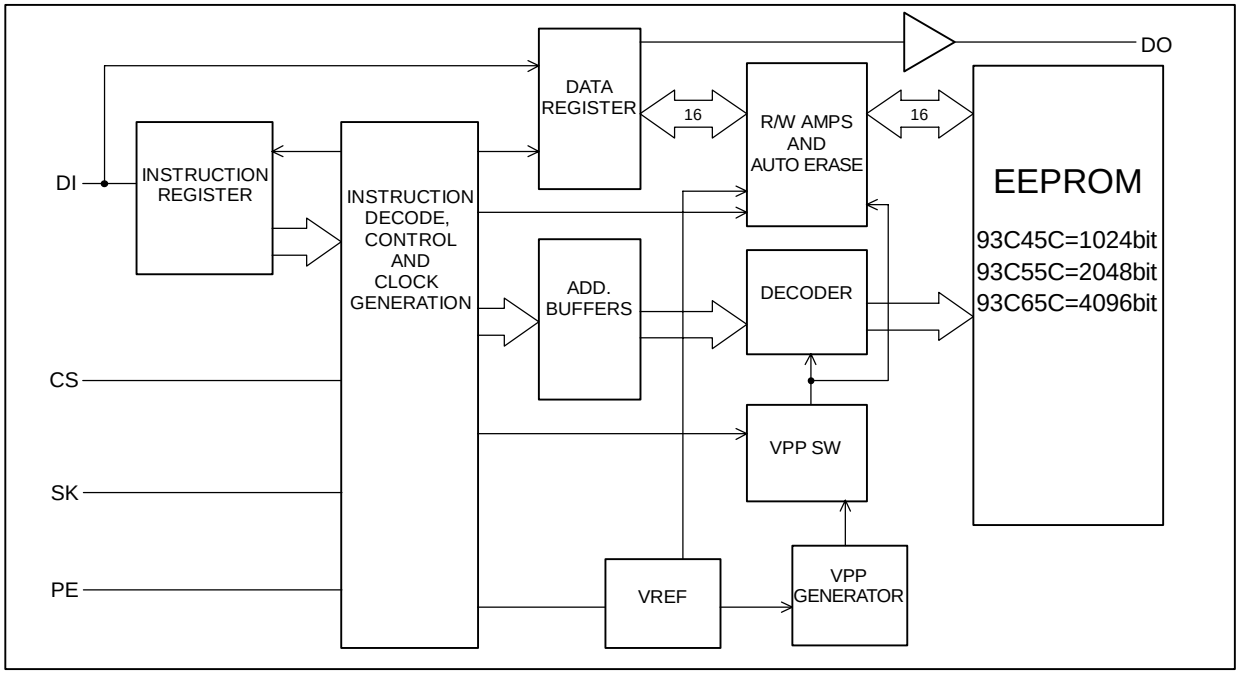
AK93C45C/55C/65C

1K/2K/4Kbit Serial CMOS EEPROM

Features

- ☐ ADVANCED CMOS EEPROM TECHNOLOGY
- ☐ READ/WRITE NON-VOLATILE MEMORY
- ☐ WIDE VCC OPERATION : VCC = 1.5V to 5.5V(READ)
  VCC = 1.6V to 5.5V(WRITE/WRAL/PAGE WRITE)
- ☐ AK93C45C ・・1024 bits, 64 x 16 organization
  AK93C55C ・・2048 bits, 128 x 16 organization
  AK93C65C ・・4096 bits, 256 x 16 organization
- ☐ SERIAL INTERFACE
  - Interfaces with popular microcontrollers and standard microprocessors
  -1.0MHz(1.5V≤VCC<2.5V), 4.0MHz(2.5V≤VCC≤5.5V)
- ☐ LOW POWER CONSUMPTION
  - 0.8μA Max. Standby
- ☐ High Reliability
  - Endurance : 1000K E/W cycles / Address
  - Data Retention : 10 years
- ☐ Automatic address increment (READ)
- ☐ Automatic write cycle time-out with auto-ERASE
- ☐ Busy/Ready status signal
- ☐ Software and Hardware controlled write protection
- ☐ IDEAL FOR LOW DENSITY DATA STORAGE
  - Low cost, space saving, 8-pin package (TMSOP, SON, USON)



Block Diagram

General Description

The AK93C45C/55C/65C is a 1024/2048/4096-bit serial CMOS EEPROM divided into 64/128/256 registers of 16 bits each. The AK93C45C/55C/65C has 6 instructions such as READ, WRITE, PAGE WRITE, EWEN, EWDS and WRAL. Those instructions control the AK93C45C/55C/65C.
The AK93C45C/55C/65C can operate full function under wide operating voltage range. The charge up circuit is integrated for high voltage generation that is used for write operation.
A serial interface of AK93C45C/55C/65C, consisting of chip select (CS), serial clock (SK), data-in (DI) and data-out (DO), can easily be controlled by popular microcontrollers or standard microprocessors. AK93C45C/55C/65C takes in the write data from data input pin (DI) to a register synchronously with rising edge of input pulse of serial clock pin (SK). And at read operation, AK93C45C/55C/65C takes out the read data from a register to data output pin (DO) synchronously with rising edge of SK.
The DO pin is usually in high impedance state. The DO pin outputs "L" or "H" in case of data output or $\overline{\text{Busy}}$/Ready signal output.

・Software controlled write protection
When VCC is applied to the part, the part automatically powers up in the ERASE/**WRITE** Disable state. In the ERASE/**WRITE** disable state, execution of WRITE, PAGE WRITE, WRAL instruction is disabled. Before WRITE, PAGE WRITE, WRAL instruction is executed, EWEN instruction must be executed. The ERASE/**WRITE** enable state continues until EWDS instruction is executed or VCC is removed from the part.
Execution of a read instruction is independent of both EWEN and EWDS instructions.
The PE is internally pulled up to VCC. If the PE is left unconnected, the part will accept WRITE, PAGE WRITE, WRAL, EWEN and EWDS instructions.

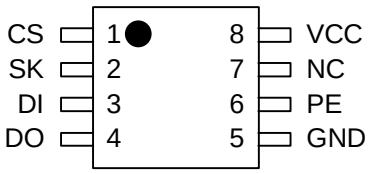
・$\overline{\text{Busy}}$/Ready status signal
After a WRITE, PAGE WRITE, WRAL instruction, the DO output serves as a $\overline{\text{Busy}}$/Ready status indicator. After the falling edge of the CS initiates the self-timed programming cycle, the DO indicates the $\overline{\text{Busy}}$/Ready status of the chip if the CS is brought high after a minimum of ‘tCS’. DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.
The $\overline{\text{Busy}}$/Ready status indicator is only valid when CS is active (high). When CS is low, the DO output goes into a high impedance state.
The $\overline{\text{Busy}}$/Ready signal outputs until a start bit (Logic"1") of the next instruction is given to the part.

■ Type of Products

Model	Memory size	Temp. Range	VCC	Package
AK93C45CT	1K bits	-40°C to +85°C	1.5V to 5.5V	8pin Plastic TMSOP
AK93C45CL		-40°C to +85°C	1.5V to 5.5V	8pin Plastic SON
AK93C45CU		-40°C to +85°C	1.5V to 5.5V	8pin Plastic USON
AK93C55CT	2K bits	-40°C to +85°C	1.5V to 5.5V	8pin Plastic TMSOP
AK93C55CL		-40°C to +85°C	1.5V to 5.5V	8pin Plastic SON
AK93C55CU		-40°C to +85°C	1.5V to 5.5V	8pin Plastic USON
AK93C65CT	4K bits	-40°C to +85°C	1.5V to 5.5V	8pin Plastic TMSOP
AK93C65CL		-40°C to +85°C	1.5V to 5.5V	8pin Plastic SON
AK93C65CU		-40°C to +85°C	1.5V to 5.5V	8pin Plastic USON

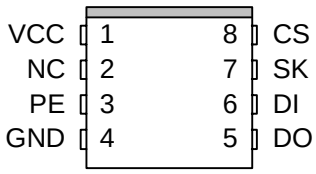
Pin Arrangement

AK93C45CT/55CT/65CT



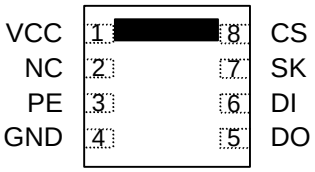
8pin TMSOP

AK93C45CL/55CL/65CL



8pin SON

AK93C45CU/55CU/65CU



8pin USON

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
PE	Program Enable
VCC	Power Supply
GND	Ground
NC	Not Connected *1

(note) The PE is internally pulled up to VCC (R = typ.2.5MΩ, VCC=5V).

*1: Please Open NC pin.

Functional Description

The AK93C45C/55C/65C has 6 instructions such as READ, WRITE, PAGE WRITE, EWEN, EWDS and WRAL. A valid instruction consists of a Start Bit (Logic"1"), the appropriate Op Code and the desired memory Address location.
The CS pin must be brought low for a minimum of 'tCS' between each instruction when the instruction is continuously executed.

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	A5-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	A5-A0	D15-D0	Writes register.
PAGE WRITE	1	11	A5-A0	D15-D0	Page Write register.
EWEN	1	00	11XXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXX		Disables all programming instructions.
WRAL	1	00	010000	D15-D0	Writes all registers.

X: Don't care

table1. Instruction Set for the AK93C45C

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	XA6-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	XA6-A0	D15-D0	Writes register.
PAGE WRITE	1	11	XA6-A0	D15-D0	Page Write register.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXXXX		Disables all programming instructions.
WRAL	1	00	010000000	D15-D0	Writes all registers.

X: Don't care

table2. Instruction Set for the AK93C55C

Instruction	Start Bit	Op Code	Address	Data	Comments
READ	1	10	A7-A0	D15-D0	Reads data stored in memory, at specified address.
WRITE	1	01	A7-A0	D15-D0	Writes register.
PAGE WRITE	1	11	A7-A0	D15-D0	Page Write register.
EWEN	1	00	11XXXXXX		Write enable must precede all programming modes.
EWDS	1	00	00XXXXXX		Disables all programming instructions.
WRAL	1	00	010000000	D15-D0	Writes all registers.

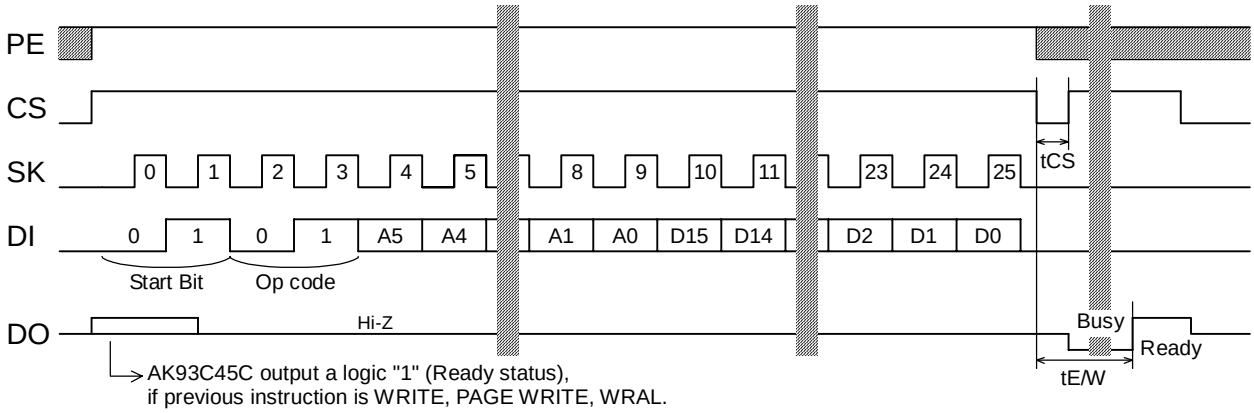
X: Don't care

table3. Instruction Set for the AK93C65C

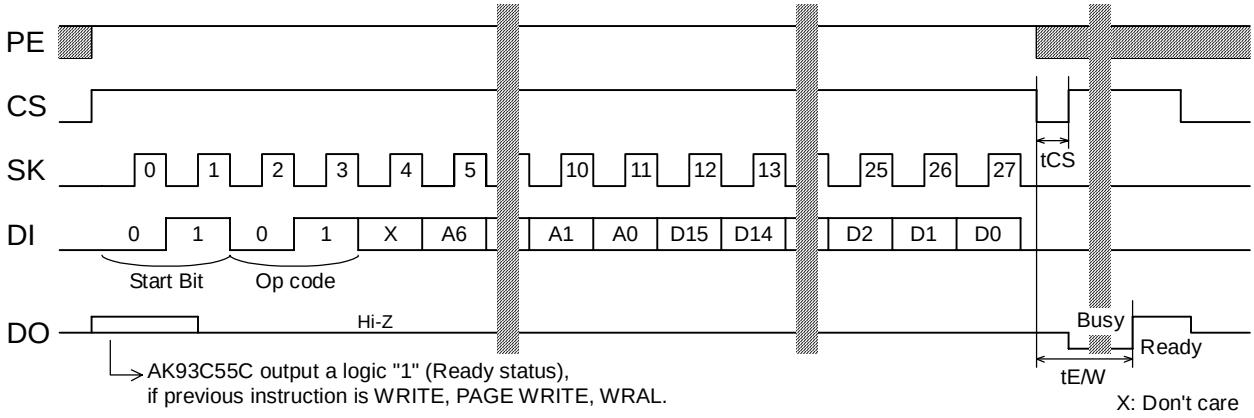
(Note) ・ The AK93C45C/55C/65C perceives the start bit in the logic"1" and also "01".

WRITE

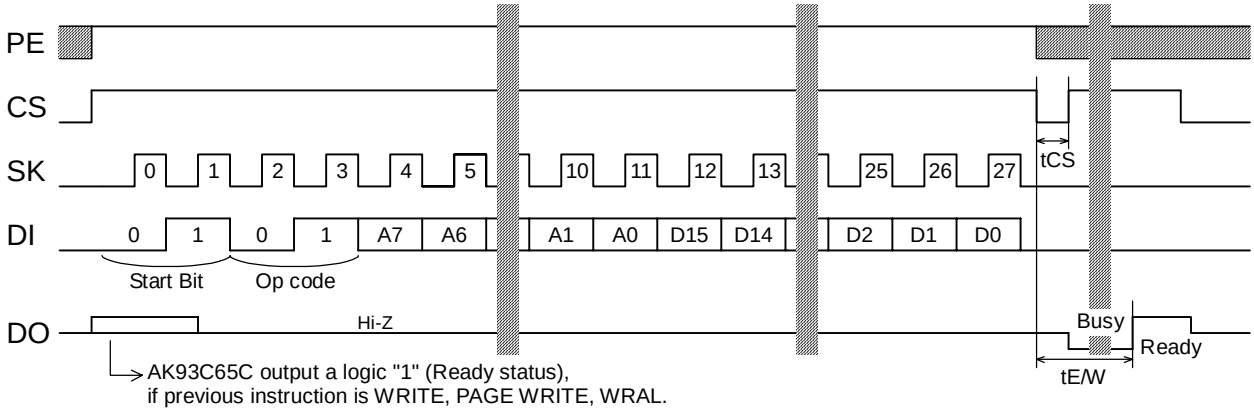
The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 'tCS'. DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.



WRITE (AK93C45C)



WRITE (AK93C55C)



WRITE (AK93C65C)

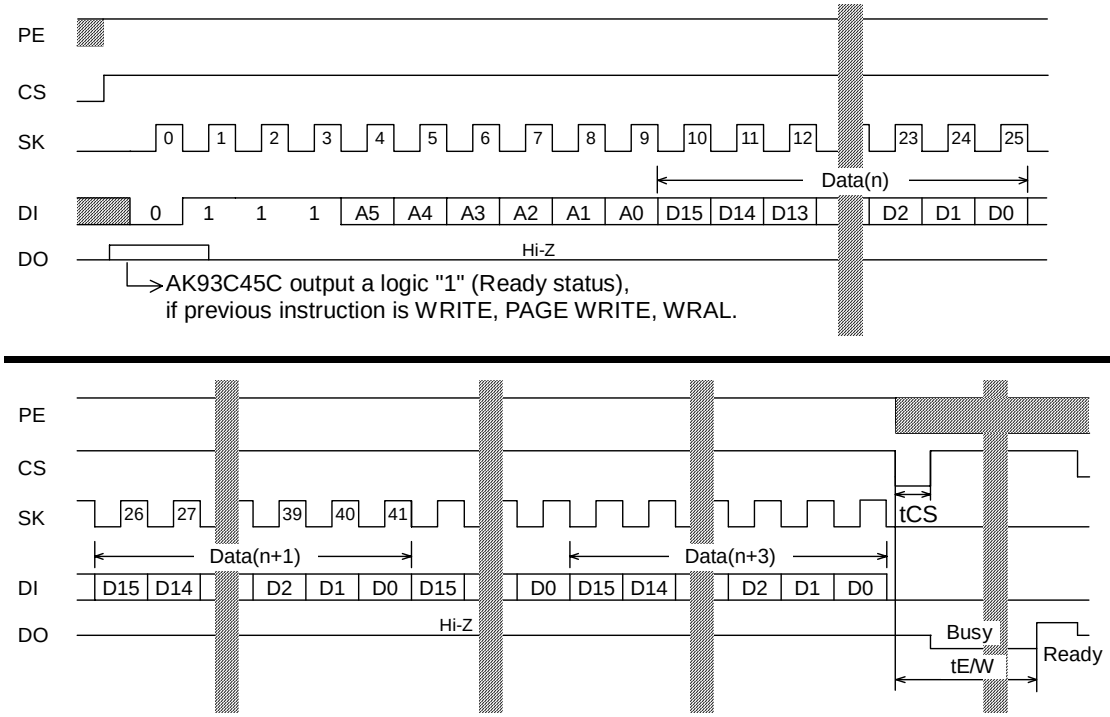
PAGE WRITE

AK93C45C/55C/65C has Page Write mode, which can write the data within 4 words with one programming cycle. The input data sent to the shift register within 4 words. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 'tCS'.

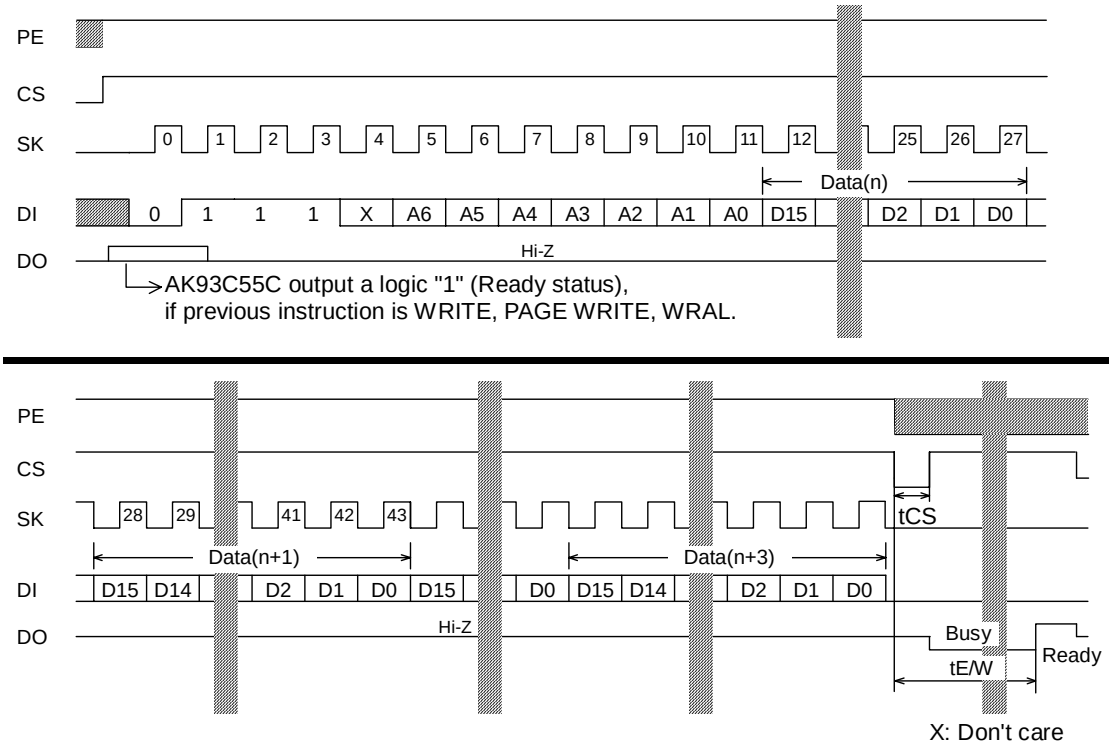
After the receipt of each word, the two lower order address pointer bits internally incremented by one. The higher order six bits of the word address remains constant. When the highest address is reached "XXXX XX11", the address counter rolls over to address "XXXX XX00" allowing the page write cycle to be continued indefinitely.

If AK93C45C/55C/65C is transmitted more than 4 words, the address counter will "roll over" and the previously written data will be overwritten. When AK93C45C/55C/65C is transmitted 6 words, fifth word will be overwritten to first word, and sixth word will be overwritten to second word.

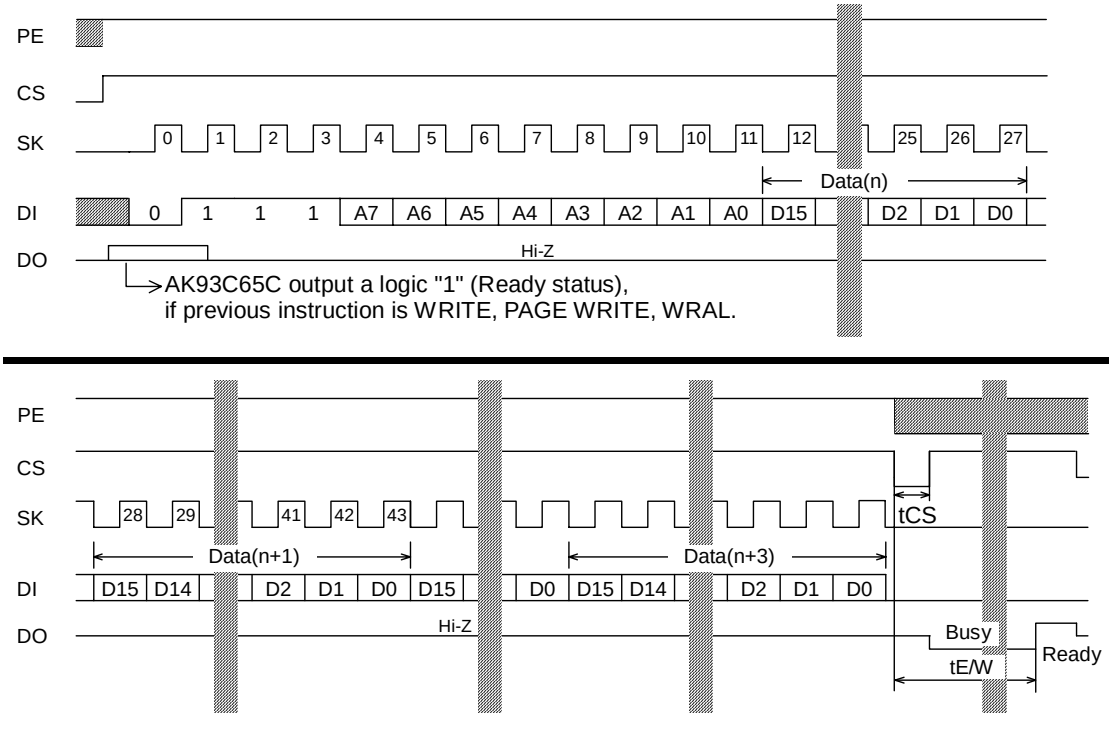
DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.



PAGE WRITE (AK93C45C)



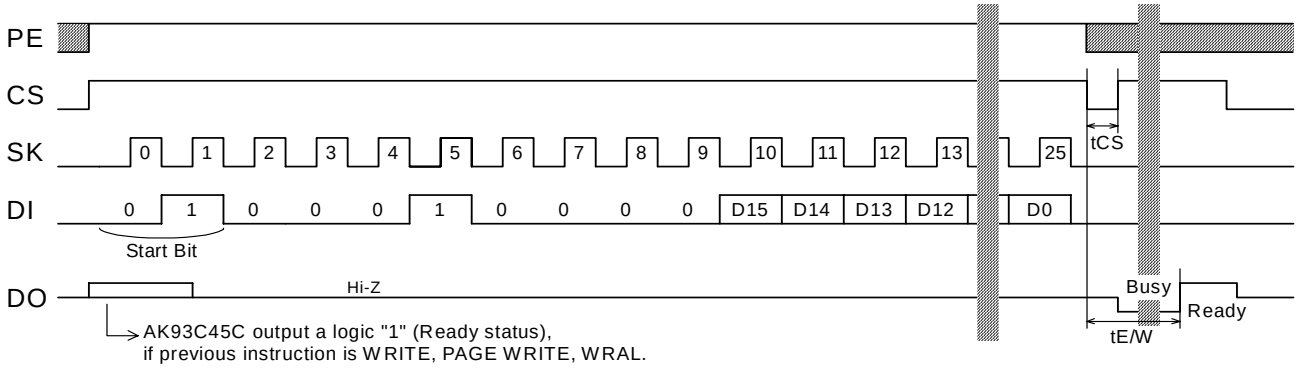
PAGE WRITE (AK93C55C)



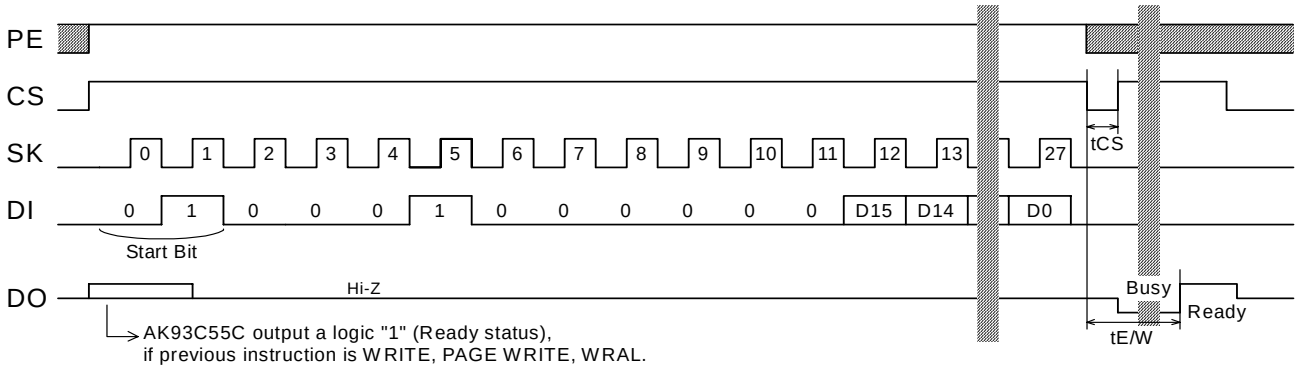
PAGE WRITE (AK93C65C)

WRAL

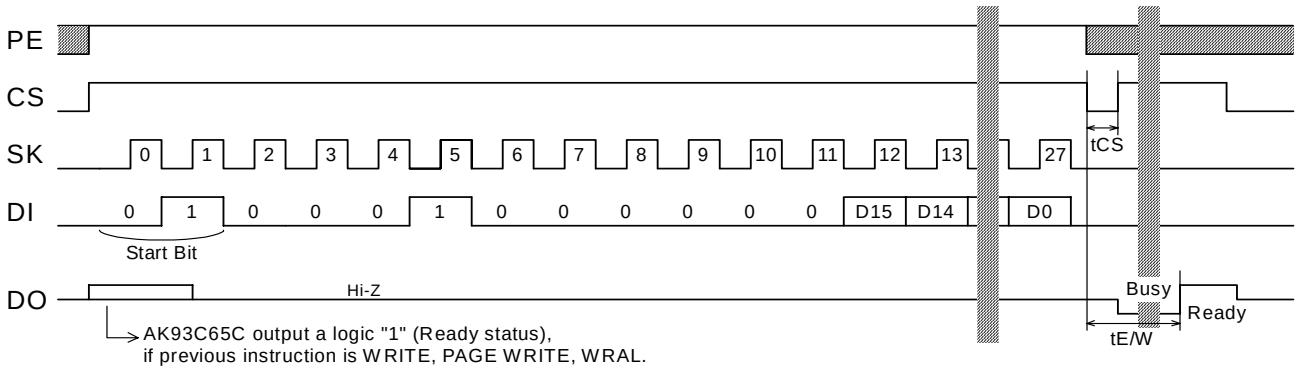
The write instruction is followed by 16 bits of data to be written into all address. After the last bit of data is put on the DI pin, the CS pin must be brought low before the next rising edge of the SK clock. This falling edge of the CS initiates the self-timed programming cycle. The DO indicates the Busy/Ready status of the chip if the CS is brought high after a minimum of 'tCS'. DO=logical "0" indicates that programming is still in progress. DO=logical "1" indicates that the register at the address specified in the instruction has been written with the new data pattern contained in the instruction and the part is ready for a next instruction.



WRAL (AK93C45C)



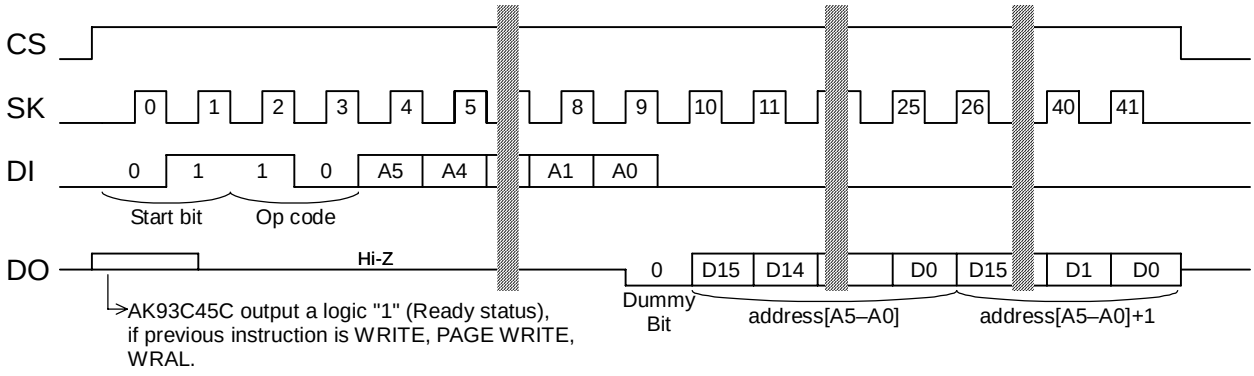
WRAL (AK93C55C)



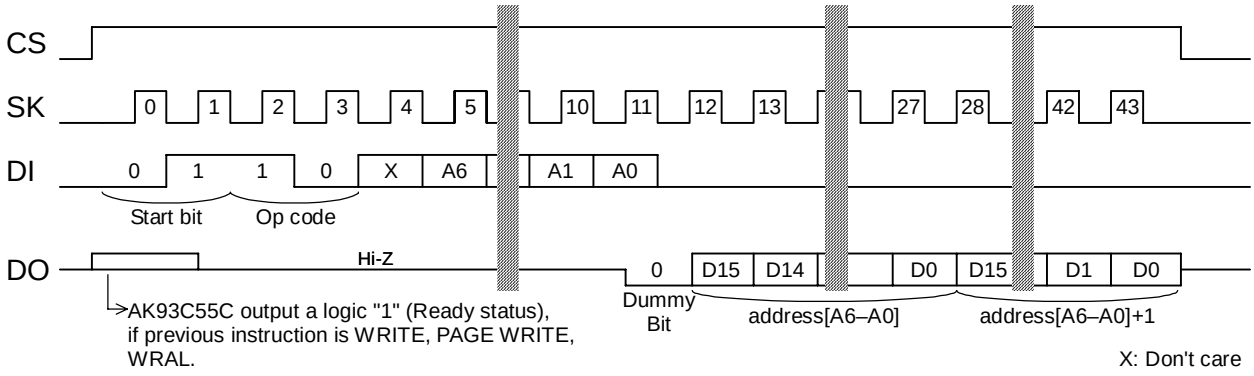
WRAL (AK93C65C)

READ

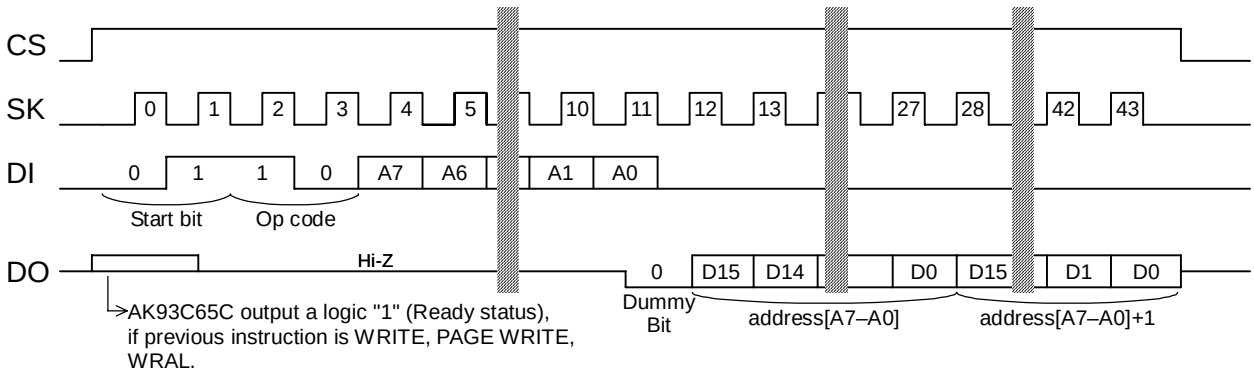
The read instruction is the only instruction which outputs serial data on the DO pin.
Following the Start bit, first Op code and address are decoded, then the data from the selected memory location is available at the DO pin. A dummy bit (logical "0") precedes the 16-bit data from the selected memory location. The output data changes are synchronized with the rising edges of the serial clock (SK).
The data in the next address can be read sequentially by continuing to provide clock. The address automatically cycles to the next higher address after the 16bit data shifted out.
When the highest address is reached, the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely.



READ (AK93C45C)



READ (AK93C55C)

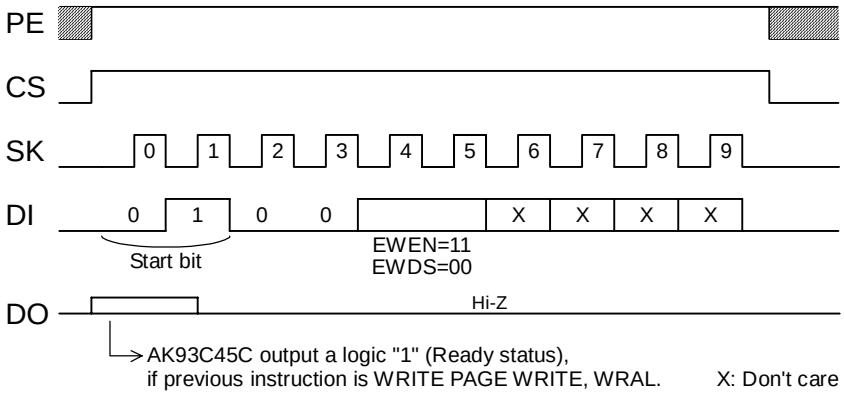


READ (AK93C65C)

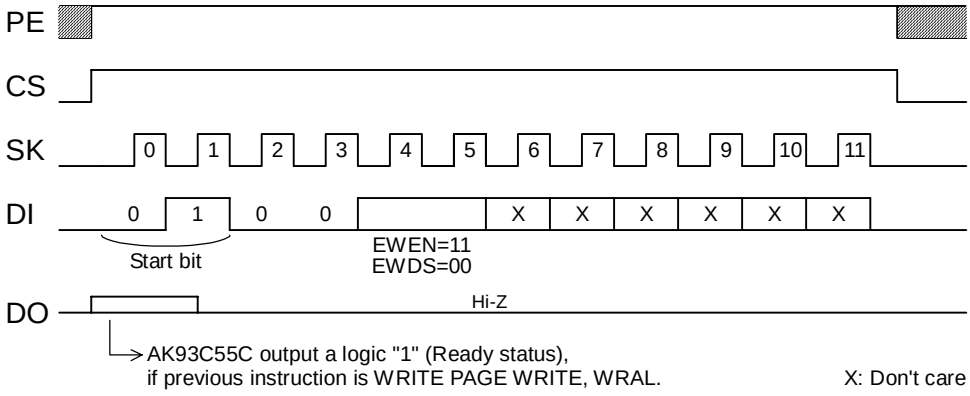
EWEN / EWDS

When VCC is applied to the part, the part automatically powers up in the ERASE/**WRITE** Disable state. In the ERASE/**WRITE** disable state, execution of WRITE, PAGE WRITE, WRAL instruction is disable. Before WRITE, PAGE WRITE, WRAL instruction is executed, EWEN instruction must be executed. The ERASE/**WRITE** enable state continues until EWDS instruction is executed or VCC is removed from the part.

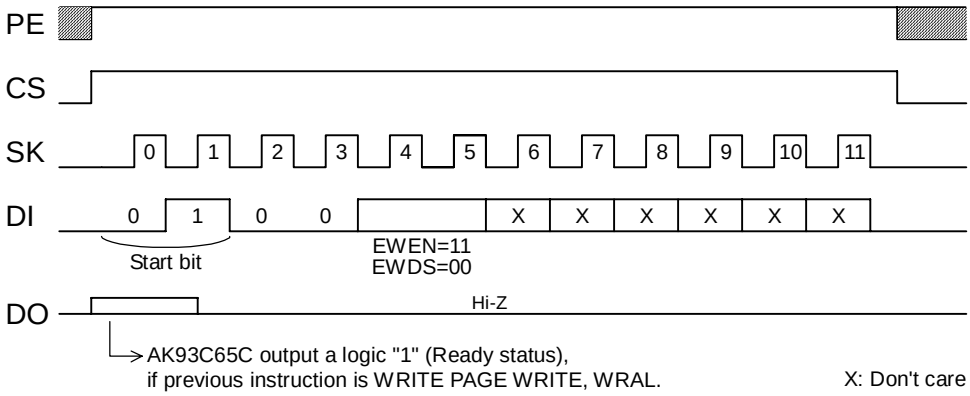
Execution of a read instruction is independent of both EWEN and EWDS instructions.



EWEN / EWDS (AK93C45C)



EWEN / EWDS (AK93C55C)



EWEN / EWDS (AK93C65C)

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply	VCC	-0.6	+6.5	V
All Input Voltages with Respect to Ground	VIO	-0.6	VCC+0.6	V
Ambient storage temperature	Tst	-65	+150	°C

Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum conditions for extended periods may affect device reliability.

Recommended Operating Condition

Parameter	Symbol	Min	Max	Unit
Power Supply 1(Except READ)	VCC1	1.6	5.5	V
Power Supply 2(READ)	VCC2	1.5	5.5	V
Ambient Operating Temperature	Ta	-40	+85	°C

Electrical Characteristics

(1) D.C. ELECTRICAL CHARACTERISTICS

(1.5V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
Current Dissipation (WRITE)	ICC1	VCC=5.5V, tSKP=250ns, *1		2.5	mA
	ICC2	VCC=1.8V, tSKP=1.0μs, *1		1.5	mA
Current Dissipation (WRAL)	ICC3	VCC=5.5V, tSKP=250ns, *1		2.5	mA
	ICC4	VCC=1.8V, tSKP=1.0μs, *1		1.5	mA
Current Dissipation (READ)	ICC5	VCC=5.5V, tSKP=250ns, *1		1.5	mA
	ICC6	VCC=1.5V, tSKP=1.0μs, *1		0.1	mA
Current Dissipation (Standby)	I_{CCSB}	VCC=5.5V *2		0.8	μA
Input High Voltage	VIH1	VCC=5.0V±10%	2.0	VCC + 0.5	V
	VIH2	2.5V ≤ VCC ≤ 5.5V	0.8 x VCC	VCC + 0.5	V
	VIH3	1.5V ≤ VCC < 2.5V	0.8 x VCC	VCC + 0.5	V
Input Low Voltage	VIL1	VCC=5.0V±10%	-0.1	0.8	V
	VIL2	1.8V ≤ VCC ≤ 5.5V	-0.1	0.15 x VCC	V
	VIL3	1.5V ≤ VCC < 1.8V	-0.1	0.1 x VCC	V
Output High Voltage	VOH1	VCC=5.0V±10% IOH=-0.4mA	2.2		V
	VOH2	2.5V ≤ VCC ≤ 5.5V IOH=-0.1mA	0.8 x VCC		V
	VOH3	1.5V ≤ VCC < 2.5V IOH=-0.1mA	0.8 x VCC		V
Output Low Voltage	VOL1	VCC=5.0V±10% IOL=1.5mA		0.4	V
	VOL2	2.5V ≤ VCC ≤ 5.5V IOL=1.0mA		0.4	V
	VOL3	1.5V ≤ VCC < 2.5V IOL=0.1mA		0.4	V
Input Leakage	ILI	VCC=5.5V, VIN=5.5V *3		±1.0	μA
Output Leakage	ILO	VCC=5.5V, VOUT=5.5V, CS=GND		±1.0	μA

*1 : VIN=VIH/VIL, DO=Open
*2 : VIN=VCC/GND, CS=GND, DO=Open, PE=VCC/Open
*3 : CS, SK, DI pin

(2) A.C. ELECTRICAL CHARACTERISTICS

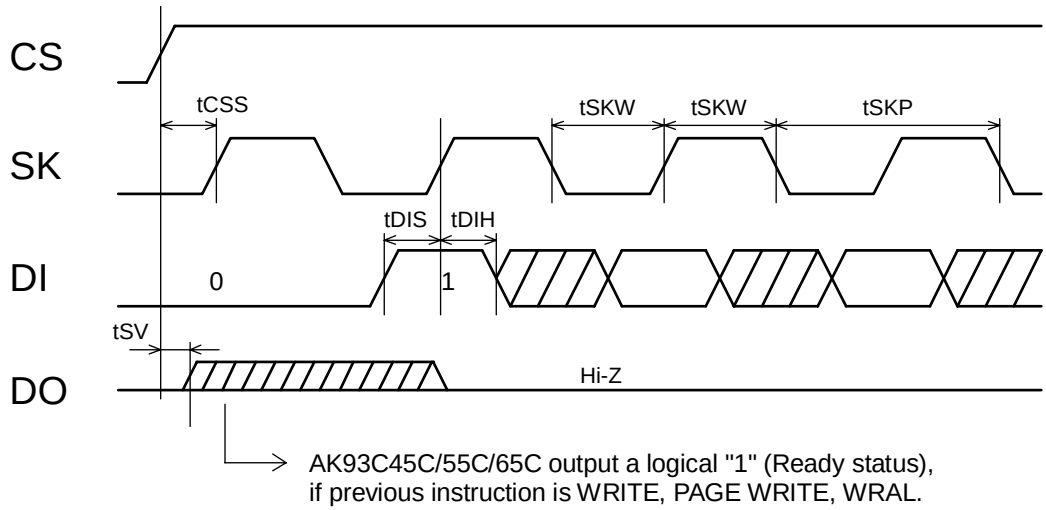
(1.5V ≤ VCC ≤ 5.5V, -40°C ≤ Ta ≤ 85°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Max.	Unit
SK Cycle Time	tSKP1	2.5V ≤ VCC ≤ 5.5V	250		ns
	tSKP2	1.5V ≤ VCC < 2.5V	1.0		μs
SK Pulse Width	tSKW1	2.5V ≤ VCC ≤ 5.5V	100		ns
	tSKW2	1.5V ≤ VCC < 2.5V	400		ns
CS Setup Time	tCSS1	2.5V ≤ VCC ≤ 5.5V	80		ns
	tCSS2	1.5V ≤ VCC < 2.5V	200		ns
CS Hold Time	tCSH		0		ns
Data Setup Time	tDIS1	2.5V ≤ VCC ≤ 5.5V	50		ns
	tDIS2	1.5V ≤ VCC < 2.5V	100		ns
Data Hold Time	tDIH1	2.5V ≤ VCC ≤ 5.5V	50		ns
	tDIH2	1.5V ≤ VCC < 2.5V	100		ns
Output delay *4	tPD1	2.5V ≤ VCC ≤ 5.5V		60	ns
	tPD2	1.5V ≤ VCC < 2.5V		300	ns
Selftimed Programming Time	tE/W	1.6V ≤ VCC ≤ 5.5V		5	ms
Min CS Low Time	tCS1	2.5V ≤ VCC ≤ 5.5V	60		ns
	tCS2	1.5V ≤ VCC < 2.5V	200		ns
SK HOLD Time	tCCH1	2.5V ≤ VCC ≤ 5.5V	60		ns
	tCCH2	1.5V ≤ VCC < 2.5V	200		ns
CS to Status Valid	tSV1	2.5V ≤ VCC ≤ 5.5V		125	ns
	tSV2	1.6V ≤ VCC < 2.5V		300	ns
CS to Output High-Z	tOZ1	2.5V ≤ VCC ≤ 5.5V		75	ns
	tOZ2	1.5V ≤ VCC < 2.5V		100	ns
Endurance *5		5.5V, 25°C, PAGE WRITE	1,000,000		E/W cycles/ Address

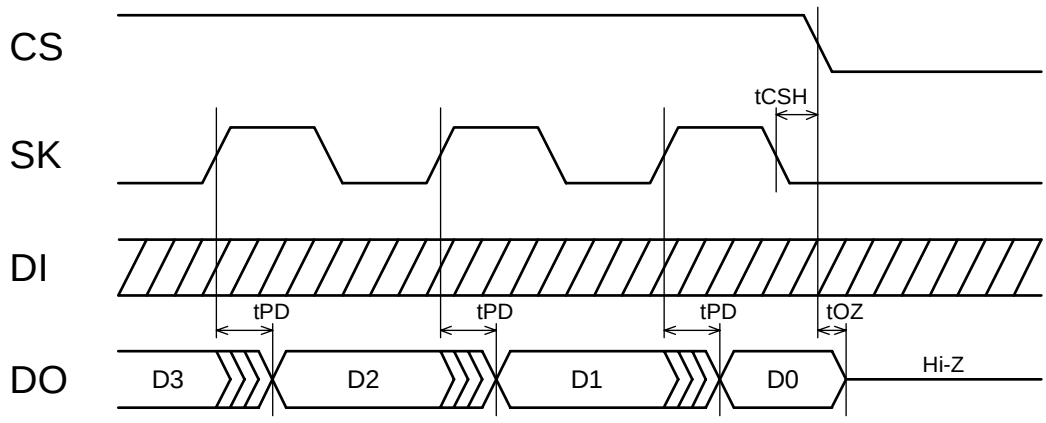
*4 : CL=100pF

*5 : This parameter is not tested to all samples.

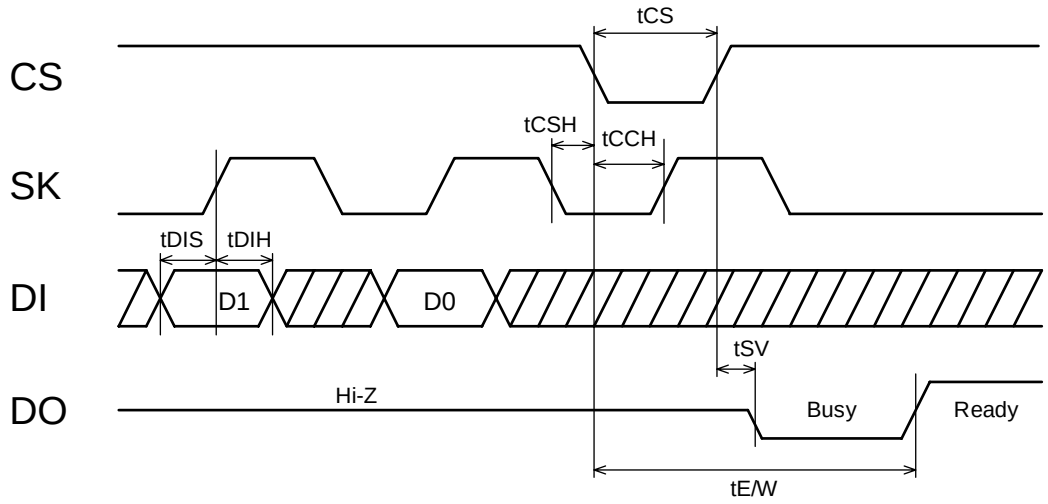
Synchronous Data timing



The Start of Instruction



The End of Instruction



$\overline{\text{Busy}}$/Ready Signal Output

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