ALPHA & OMEGA SEMICONDUCTOR, LTD

Rev 3: May 2004

# AO3415
# P-Channel Enhancement Mode Field Effect Transistor

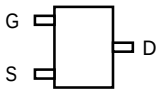
## General Description

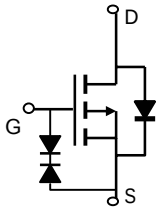
The AO3415 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected. *AO3415 is Pb-free (meets ROHS & Sony 259 specifications). AO3415L is a Green Product ordering option. AO3415 and AO3415L are electrically identical.*

## Features

$V_{DS}$ (V) = -20V
$I_D$ = -4 A
$R_{DS(ON)}$ < 43mΩ ($V_{GS}$ = -4.5V)
$R_{DS(ON)}$ < 54mΩ ($V_{GS}$ = -2.5V)
$R_{DS(ON)}$ < 73mΩ ($V_{GS}$ = -1.8V)
ESD Rating: 3000V HBM

**TO-236**
**(SOT-23)**
**Top View**




**Absolute Maximum Ratings $T_A$=25°C unless otherwise noted**

| Parameter | | Symbol | Maximum | Units |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ±8 | V |
| Continuous Drain Current [A] | $T_A$=25°C | $I_D$ | -4.0 | A |
| | $T_A$=70°C | | -3.5 | |
| Pulsed Drain Current [B] | | $I_{DM}$ | -30 | |
| Power Dissipation [A] | $T_A$=25°C | $P_D$ | 1.4 | W |
| | $T_A$=70°C | | 0.9 | |
| Junction and Storage Temperature Range | | $T_J$, $T_{STG}$ | -55 to 150 | °C |

**Thermal Characteristics**

| Parameter | | Symbol | Typ | Max | Units |
|---|---|---|---|---|---|
| Maximum Junction-to-Ambient [A] | t ≤ 10s | $R_{\theta JA}$ | 65 | 90 | °C/W |
| Maximum Junction-to-Ambient [A] | Steady-State | | 85 | 125 | °C/W |
| Maximum Junction-to-Lead [C] | Steady-State | $R_{\theta JL}$ | 43 | 60 | °C/W |

## Electrical Characteristics ($T_J$=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **STATIC PARAMETERS** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $I_D$=-250µA, $V_{GS}$=0V | -20 | | | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$=-16V, $V_{GS}$=0V | | | -1 | µA |
| | | $T_J$=55°C | | | -5 | |
| $I_{GSS}$ | Gate-Body leakage current | $V_{DS}$=0V, $V_{GS}$=±4.5V | | | ±1 | µA |
| | | $V_{DS}$=0V, $V_{GS}$=±8V | | | ±10 | µA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$ $I_D$=-250µA | -0.3 | -0.55 | -1 | |
| $I_{D(ON)}$ | On state drain current | $V_{GS}$=-4.5V, $V_{DS}$=-5V | -25 | | | A |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance | $V_{GS}$=-4.5V, $I_D$=-4A | | 35 | 43 | mΩ |
| | | $T_J$=125°C | | 48 | 60 | |
| | | $V_{GS}$=-2.5V, $I_D$=-4A | | 45 | 54 | mΩ |
| | | $V_{GS}$=-1.8V, $I_D$=-2A | | 56 | 73 | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$=-5V, $I_D$=-4A | 8 | 16 | | S |
| $V_{SD}$ | Diode Forward Voltage | $I_S$=-1A,$V_{GS}$=0V | | -0.78 | -1 | V |
| $I_S$ | Maximum Body-Diode Continuous Current | | | | -2.2 | A |
| **DYNAMIC PARAMETERS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-10V, f=1MHz | | 1450 | | pF |
| $C_{oss}$ | Output Capacitance | | | 205 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 160 | | pF |
| $R_g$ | Gate resistance | $V_{GS}$=0V, $V_{DS}$=0V, f=1MHz | | 6.5 | | Ω |
| **SWITCHING PARAMETERS** | | | | | | |
| $Q_g$ | Total Gate Charge | $V_{GS}$=-4.5V, $V_{DS}$=-10V, $I_D$=-4A | | 17.2 | | nC |
| $Q_{gs}$ | Gate Source Charge | | | 1.3 | | nC |
| $Q_{gd}$ | Gate Drain Charge | | | 4.5 | | nC |
| $t_{D(on)}$ | Turn-On DelayTime | $V_{GS}$=-4.5V, $V_{DS}$=-10V, $R_L$=2.5Ω, $R_{GEN}$=3Ω | | 9.5 | | ns |
| $t_r$ | Turn-On Rise Time | | | 17 | | ns |
| $t_{D(off)}$ | Turn-Off DelayTime | | | 94 | | ns |
| $t_f$ | Turn-Off Fall Time | | | 35 | | ns |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$=-4A, dI/dt=100A/µs | | 31 | | ns |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | $I_F$=-4A, dI/dt=100A/µs | | 13.8 | | nC |

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25°C. The SOA curve provides a single pulse rating.

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

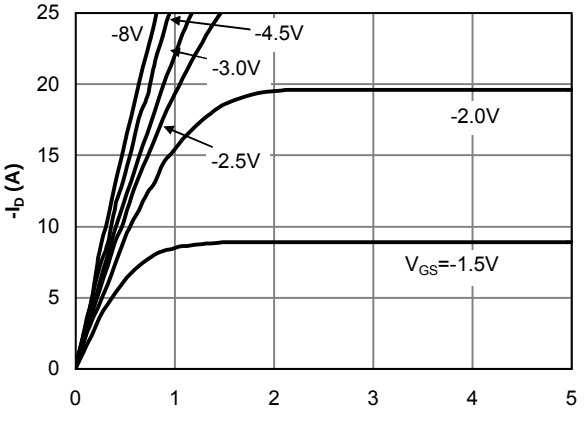



**Fig 1: On-Region Characteristics**

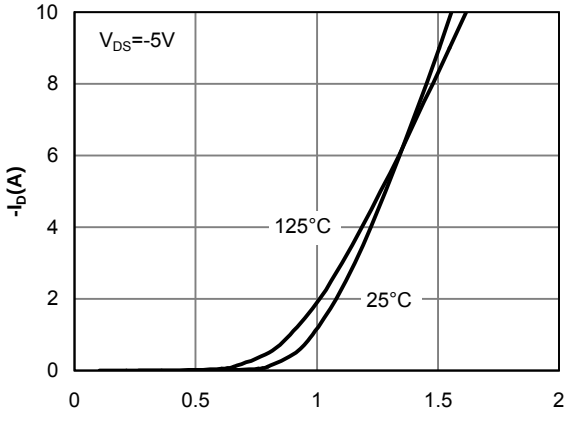



**Figure 2: Transfer Characteristics**

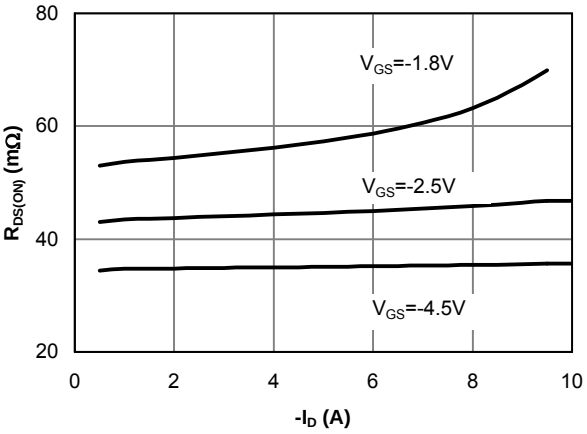



**Figure 3: On-Resistance vs. Drain Current and Gate Voltage**

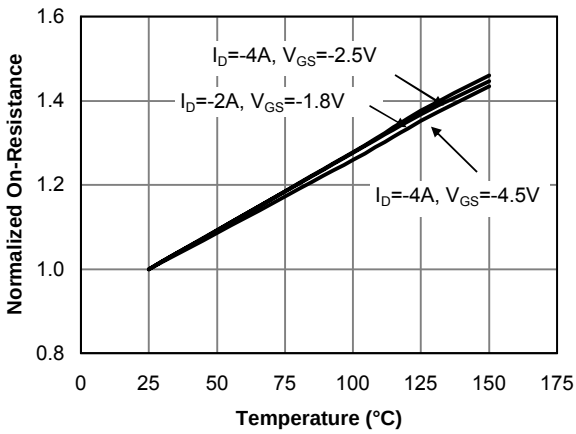



**Figure 4: On-Resistance vs. Junction Temperature**

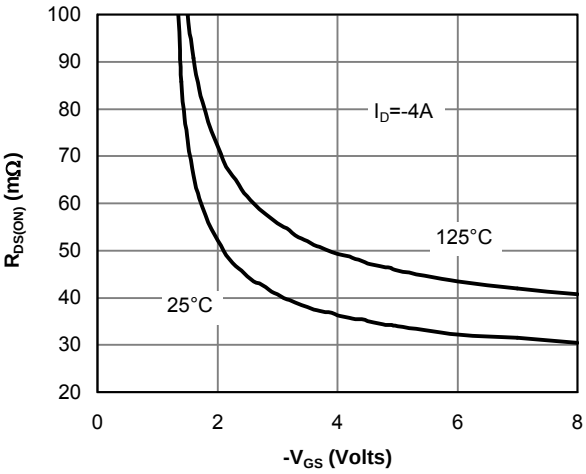



**Figure 5: On-Resistance vs. Gate-Source Voltage**

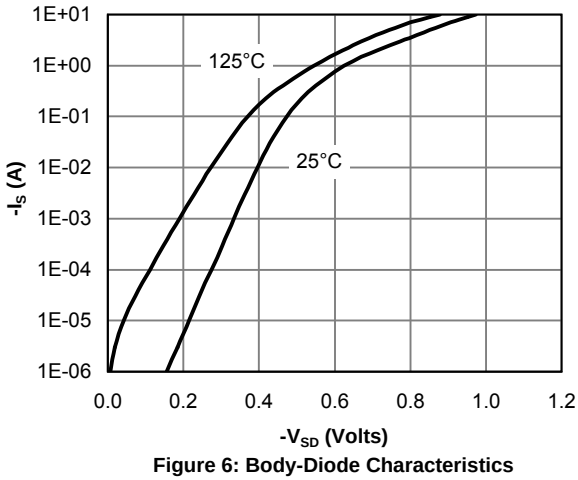



**Figure 6: Body-Diode Characteristics**

## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

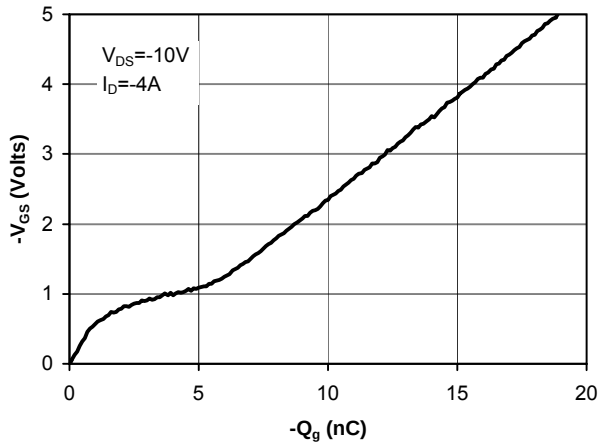



**Figure 7: Gate-Charge Characteristics**

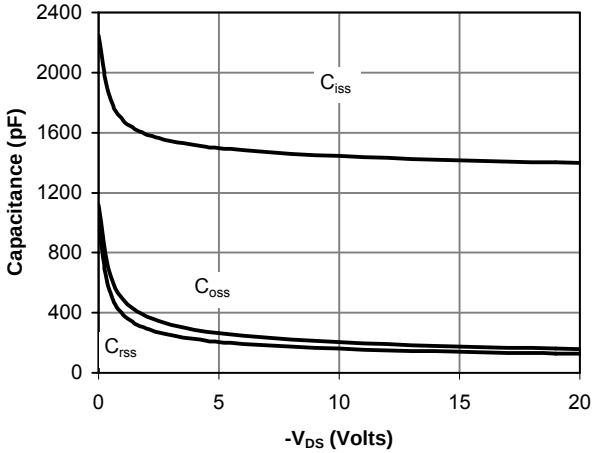



**Figure 8: Capacitance Characteristics**

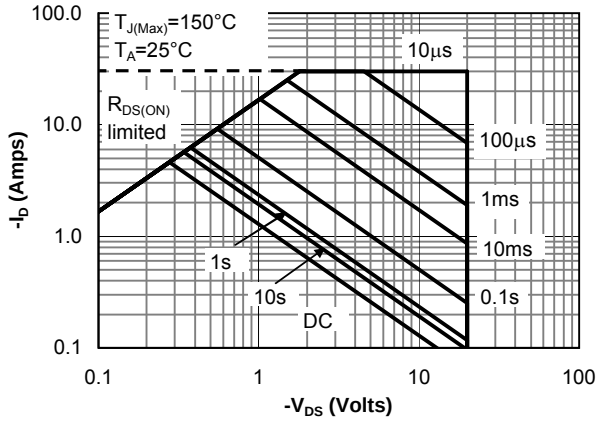



**Figure 9: Maximum Forward Biased Safe Operating Area (Note E)**

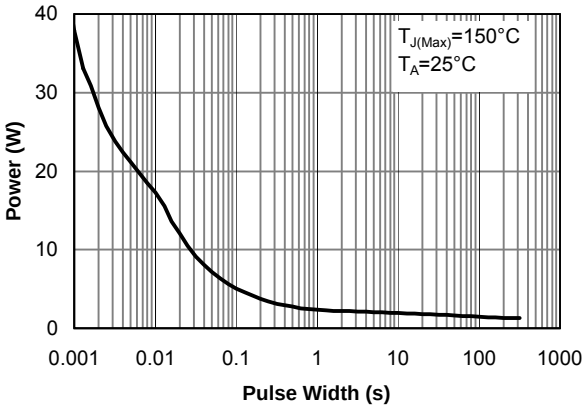



**Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)**

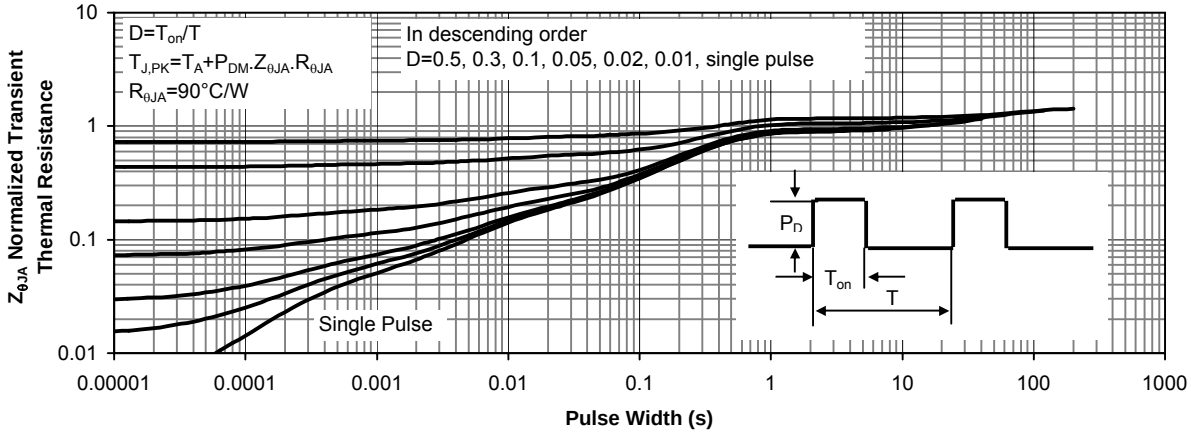



**Figure 11: Normalized Maximum Transient Thermal Impedance**