

3SK181



2046

T-31-25

N-Channel Enhancement
MOS Silicon FET(Dual Gate)

High-Frequency General-Purpose Amp Applications

©2130A

Applications

- FM tuners and VHF tuners

Features

- Enhancement type
- Easy AGC (Cut off at $V_{G2S}=0V$)
- High power gain and low noise figure
- High forward transfer admittance

Absolute Maximum Ratings at $T_a=25^\circ C$

		unit
Drain to Source Voltage	V_{DS}	15 V
Gate 1 to Source Voltage	V_{G1S}	± 10 V
Gate 2 to Source Voltage	V_{G2S}	± 10 V
Drain Current	I_D	30 mA
Power Dissipation	P_D	200 mW
Channel Temperature	T_{ch}	125 $^\circ C$
Storage Temperature	T_{stg}	-55 to +125 $^\circ C$

Electrical Characteristics at $T_a=25^\circ C$

			min	typ	max	unit
Drain to Source Voltage	V_{DS}	$V_{G1S}=0V, V_{G2S}=0V$	15			V
		$I_{DS}=100\mu A$				
Gate 1 to Source Breakdown Voltage	$V(BR)_{G1SS}$	$I_{G1}=10\mu A, V_{DS}=0V, V_{G2S}=0V$	± 10			V
Gate 2 to Source Breakdown Voltage	$V(BR)_{G2SS}$	$I_{G2}=10\mu A, V_{DS}=0V, V_{G1S}=0V$	± 10			V
Gate 1 to Source Cutoff Voltage	$V_{G1S}(off)$	$V_{DS}=10V, V_{G2S}=6V, I_D=100\mu A$	0	0.7	1.3	V
Gate 2 to Source Cutoff Voltage	$V_{G2S}(off)$	$V_{DS}=10V, V_{G1S}=3V, I_D=100\mu A$	0.1	0.9	1.6	V
Gate 1 Cutoff Current	I_{G1SS}	$V_{G1S}=4V, V_{G2S}=V_{DS}=0V$			50	nA
Gate 2 Cutoff Current	I_{G2SS}	$V_{G2S}=8V, V_{G1S}=V_{DS}=0V$			50	nA
Drain Current	I_{DSX}	$V_{DS}=10V, V_{G1S}=1.5V, V_{G2S}=6V$	2.5*		24*	mA

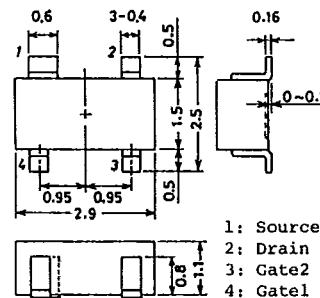
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*: The 3SK181 is classified by I_{DSX} as follows (unit:mA):

2.5	4	6.0	5.0	5	12.0	10.0	6	24.0
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(Note) Marking: EJ
 I_{DSX} rank : 4,5,6

Case Outline 2046
(unit:mm)

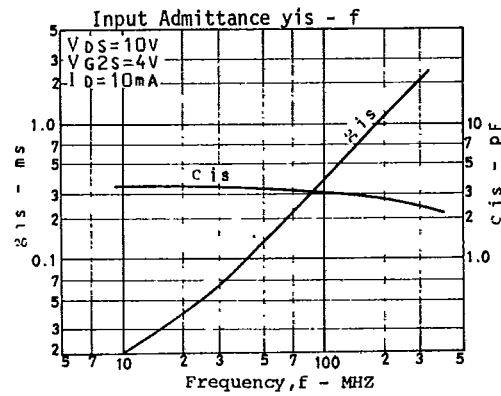
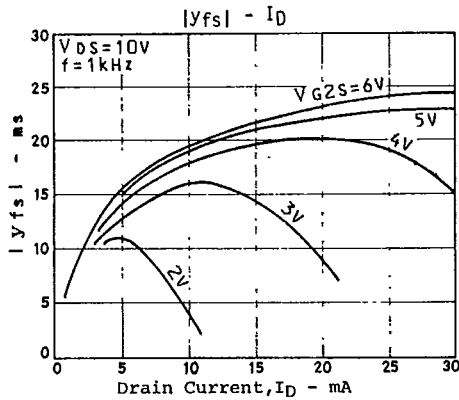
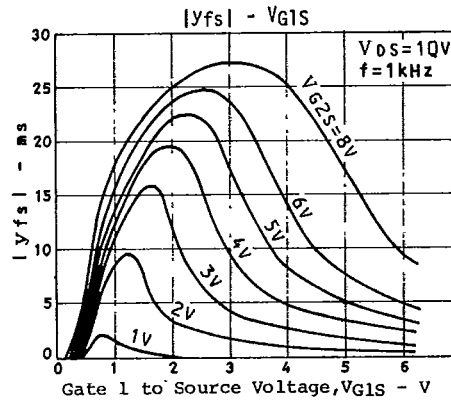
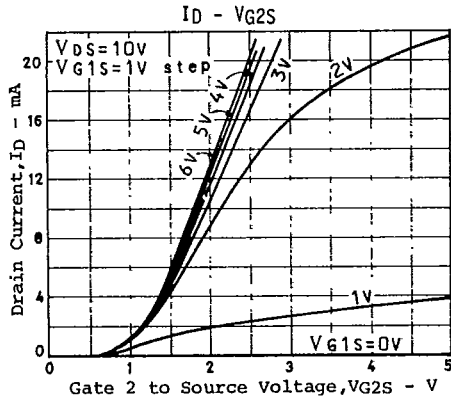
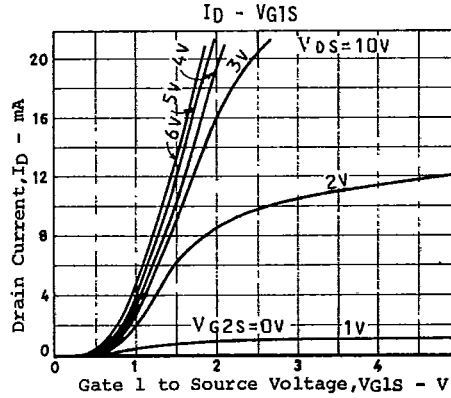
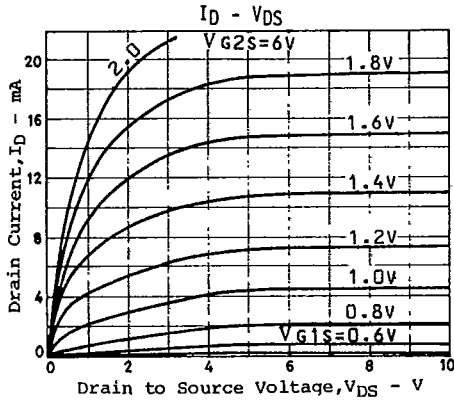


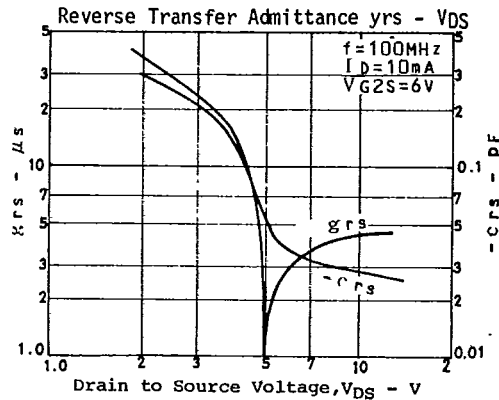
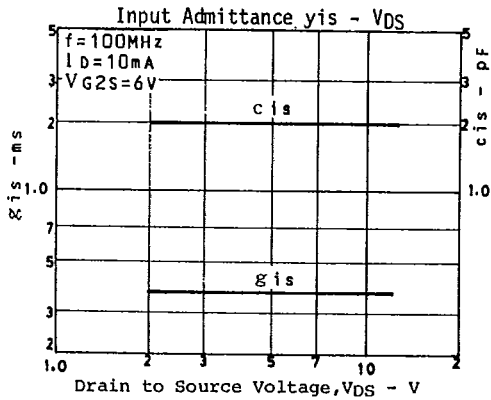
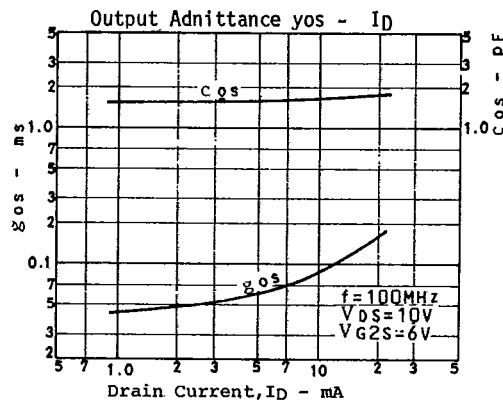
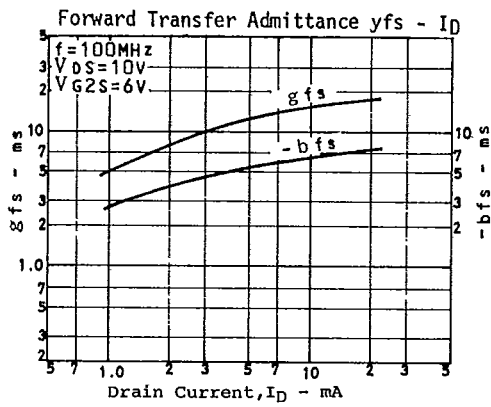
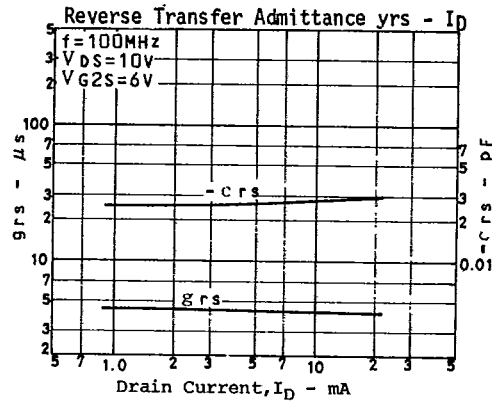
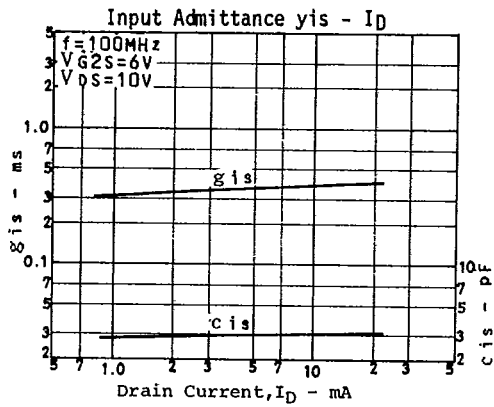
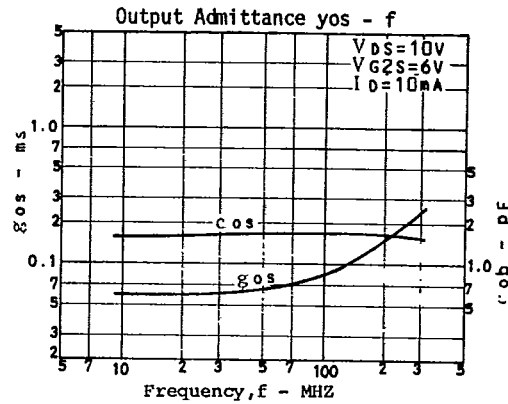
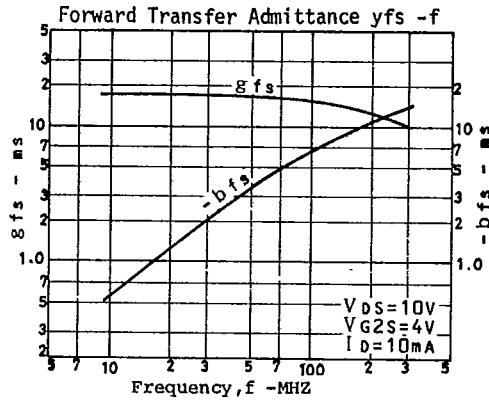
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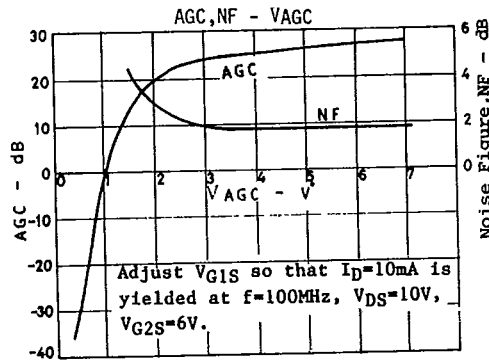
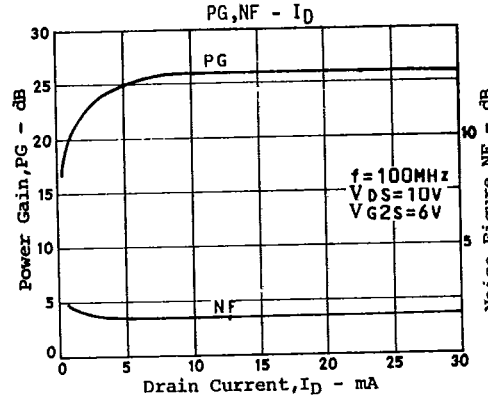
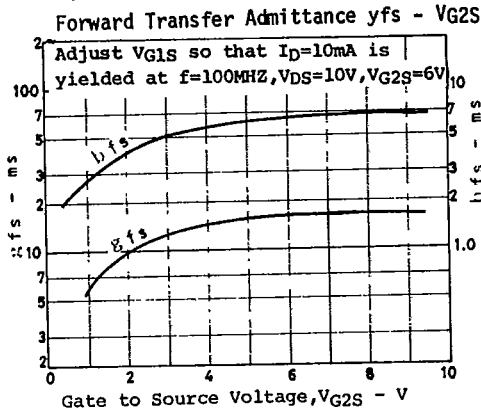
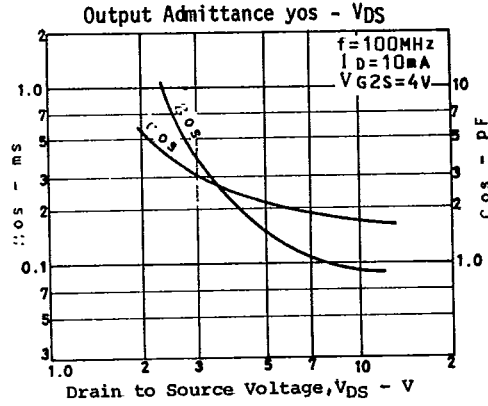
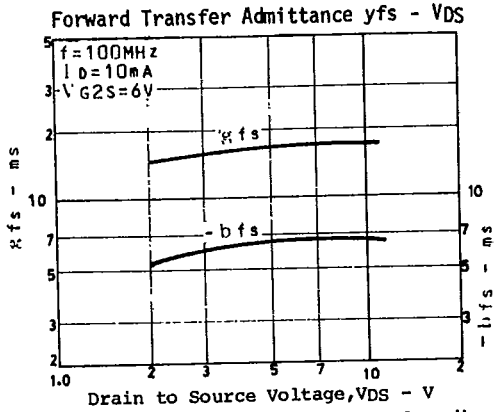
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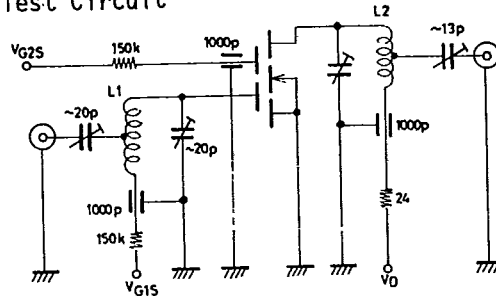
			min	typ	max	unit
Forward Transfer Admittance	$ y_{fs} $	$f=1\text{kHz}, I_D=10\text{mA}$ $V_{DS}=10\text{V}, V_{G2S}=6\text{V}$		18		ms
Input Capacitance	C_{iss}	$V_{DS}=10\text{V}, f=1\text{MHz}$ $V_{G1S}=0\text{V}, V_{G2S}=6\text{V}$		3.0		pF
Reverse Transfer Capacitance	C_{rss}			0.02	0.05	pF
Power Gain	PG	$V_{DS}=10\text{V}, I_D=10\text{mA}$	22	28		dB
Noise Figure	NF	$f=100\text{MHz}, V_{G2S}=6\text{V}$		1.8	3.0	dB







PG, NF Test Circuit

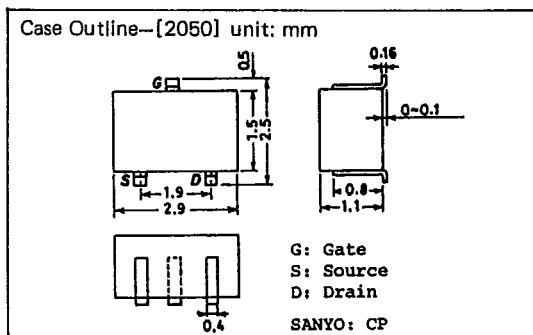
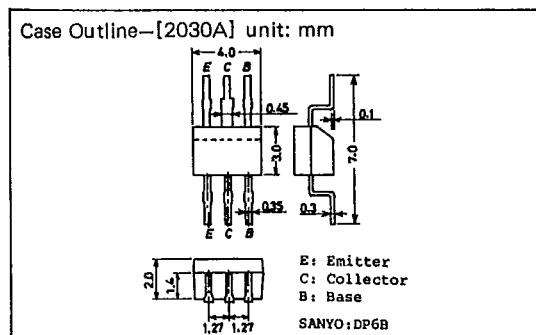
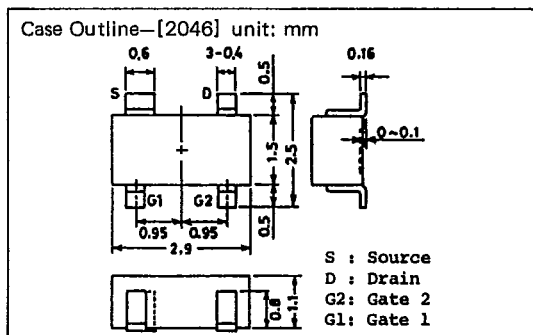
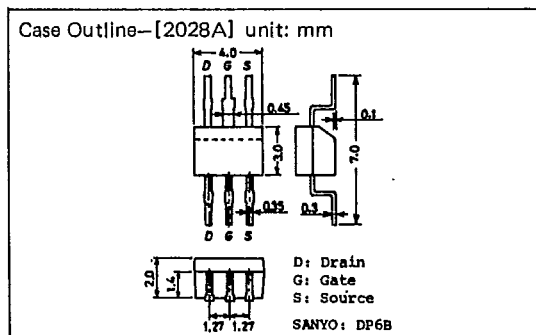
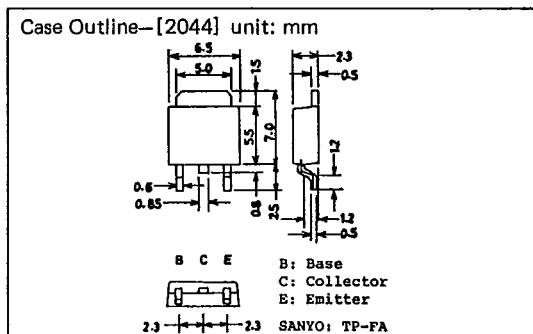
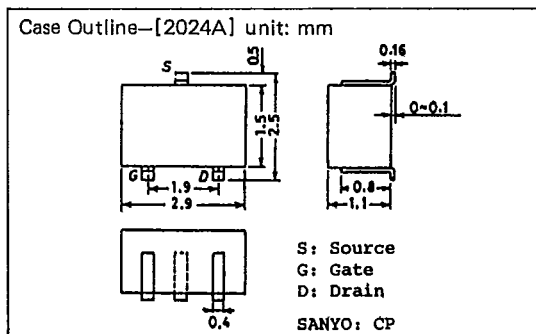
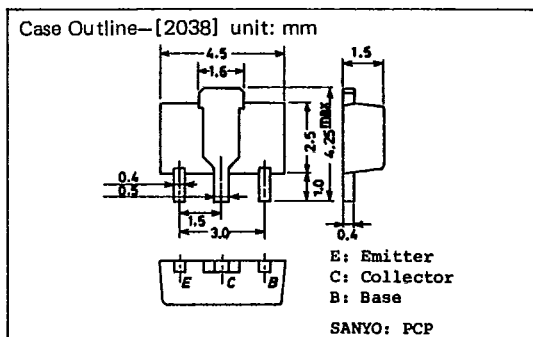
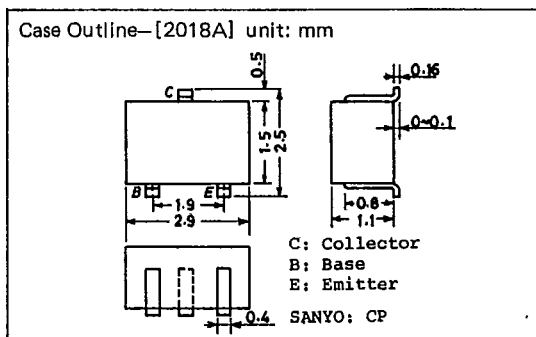


L1: 1mm ϕ plated wire 10mm ϕ 4T, tap: 1T from gate side.
 L2: 1mm ϕ plated wire 10mm ϕ 6T, tap: 1T from drain side.

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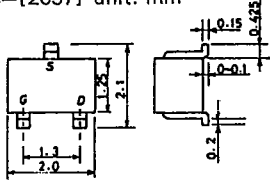
CASE OUTLINES OF SURFACE MOUNT TRANSISTORS

- All of Sanyo surface mount transistor case outlines are illustrated below.
- All dimensions are in mm, and dimensions which are not followed by min. or max. are represented by typical values.
- No marking is indicated.



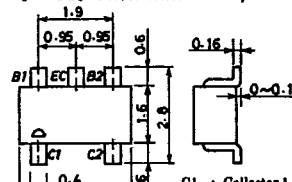
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Case Outline—[2057] unit: mm



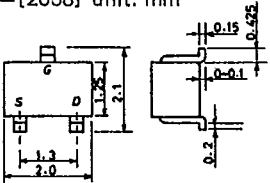
S: Source
G: Gate
D: Drain
SANYO: MCP

Case Outline—[2066] unit: mm



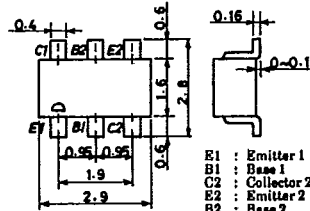
C1 : Collector 1
C2 : Collector 2
B2 : Base 2
EC : Emitter Common
B1 : Base 1
SANYO : CP6

Case Outline—[2058] unit: mm



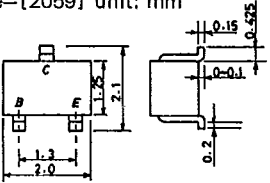
G: Gate
S: Source
D: Drain
SANYO: MCP

Case Outline—[2067] unit: mm



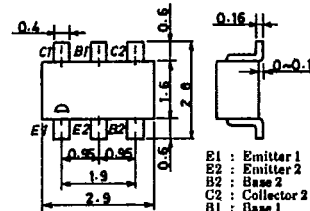
E1 : Emitter 1
B1 : Base 1
C2 : Collector 2
E2 : Emitter 2
B2 : Base 2
C1 : Collector 1
SANYO : CP6

Case Outline—[2059] unit: mm



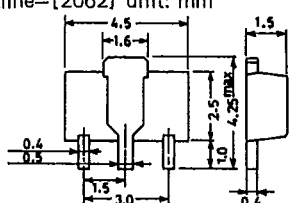
B: Base
C: Collector
E: Emitter
SANYO: MCP

Case Outline—[2068] unit: mm



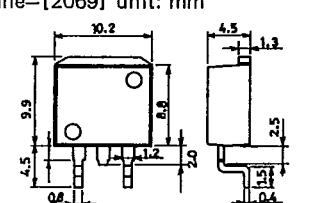
B1 : Emitter 1
E2 : Emitter 2
B2 : Base 2
C2 : Collector 2
B1 : Base 1
C1 : Collector 1
SANYO : CP6

Case Outline—[2062] unit: mm



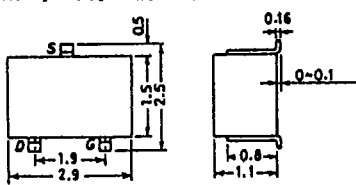
S: Source
D: Drain
G: Gate
SANYO: PCP

Case Outline—[2069] unit: mm



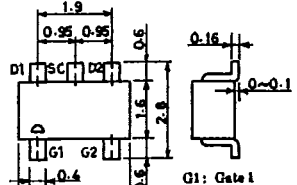
B: Base
C: Collector
E: Emitter
SANYO: SMP

Case Outline—[2065] unit: mm



S: Source
D: Drain
G: Gate
SANYO: CP

Case Outline—[2070] unit: mm



G1 : Gate 1
G2 : Gate 2
D2 : Drain 2
SC : Source Common
D1 : Drain 1
SANYO : CP6

T-9120

