

# HD74HCT245

## Octal Bus Transceivers (with 3-state outputs)

REJ03D0665-0200  
(Previous ADE-205-554)  
Rev.2.00  
Mar 30, 2006

### Description

This device has an active low enable input  $\overline{G}$  and a direction control input (DIR). When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The HD74HCT245 transfers true data from one bus to the other.

This device does not have schmitt trigger inputs.

### Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation:  $t_{pd}$  (A to Y) = 12 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 4.5$  to  $5.5$  V
- Low Input Current:  $1 \mu A$  max
- Low Quiescent Supply Current:  $I_{CC}$  (static) =  $4 \mu A$  max ( $T_a = 25^\circ C$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC245P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HC245FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HC245RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HC245TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

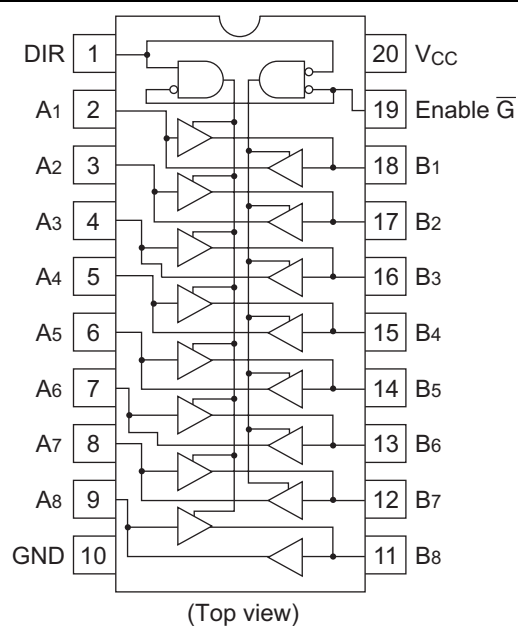
Note: Please consult the sales office for the above package availability.

### Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H : high level  
L : low level  
X : irrelevant

## Pin Arrangement



## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_O$	$\pm 35$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 75$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

## Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	4.5 to 5.5	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	°C	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 500	ns	$V_{CC} = 4.5$ V

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

## Electrical Characteristics

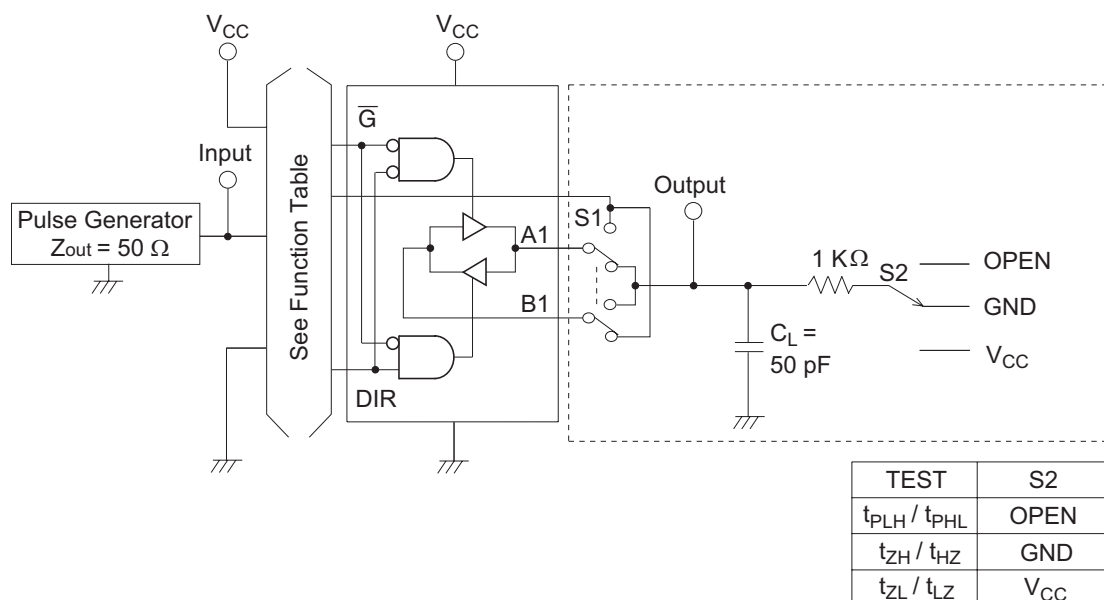
Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V <sub>IH</sub>	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V <sub>IL</sub>	4.5 to 5.5	—	—	0.8	—	0.8	V		
Output voltage	V <sub>OH</sub>	4.5	4.4	—	—	4.4	—	V	Vin = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA
		4.5	4.18	—	—	4.13	—			I <sub>OH</sub> = -6 mA
	V <sub>OL</sub>	4.5	—	—	0.1	—	0.1	V	Vin = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA
		4.5	—	—	0.26	—	0.33			I <sub>OL</sub> = 6 mA
Off-state output current	I <sub>OZ</sub>	5.5	—	—	±0.5	—	±5.0	μA	Vin = V <sub>IH</sub> or V <sub>IL</sub> , Vout = V <sub>CC</sub> or GND	
Input current	I <sub>in</sub>	5.5	—	—	±0.1	—	±1.0	μA	Vin = V <sub>CC</sub> or GND	
Quiescent current	I <sub>CC</sub>	5.5	—	—	4.0	—	40	μA	Vin = V <sub>CC</sub> or GND, Iout = 0 μA	

## Switching Characteristics

(C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

Item	Symbol	V <sub>CC</sub> (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t <sub>PLH</sub>	4.5	—	11	22	—	28	ns	
	t <sub>PHL</sub>	4.5	—	13	22	—	28		
Output enable time	t <sub>ZL</sub>	4.5	—	17	30	—	38	ns	
	t <sub>ZH</sub>	4.5	—	14	30	—	38		
Output disable time	t <sub>LZ</sub>	4.5	—	20	30	—	38	ns	
	t <sub>HZ</sub>	4.5	—	22	30	—	38		
Output rise/fall time	t <sub>TLH</sub>	4.5	—	4	12	—	15	ns	
	t <sub>THL</sub>	4.5	—	4	12	—	15		
Input capacitance	C <sub>in</sub>	—	—	5	10	—	10	pF	

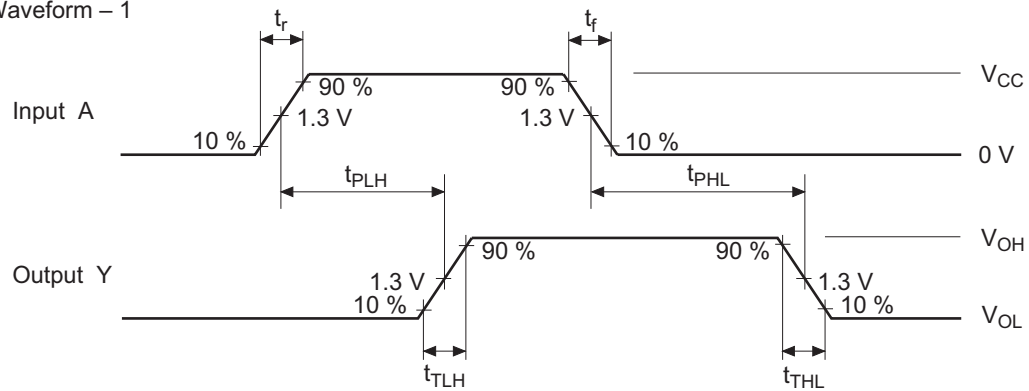
## Test Circuit



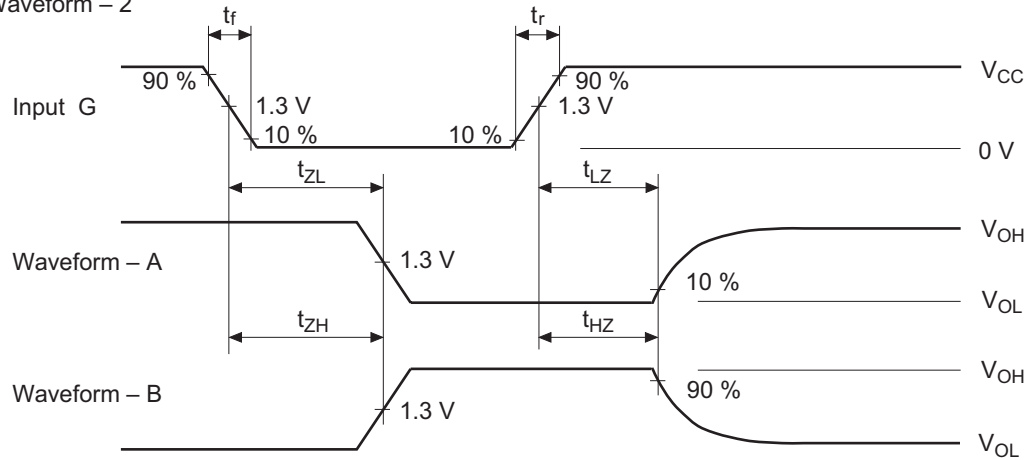
- Note : 1. C<sub>L</sub> includes probe and jig capacitance.  
 2. A2-B2, A3-B3, A4-B4, A5-B5, A6-B6, A7-B7, A8-B8 are identical to above load circuit.  
 3. S1 is a input / output switch.

## Waveforms

## • Waveform – 1

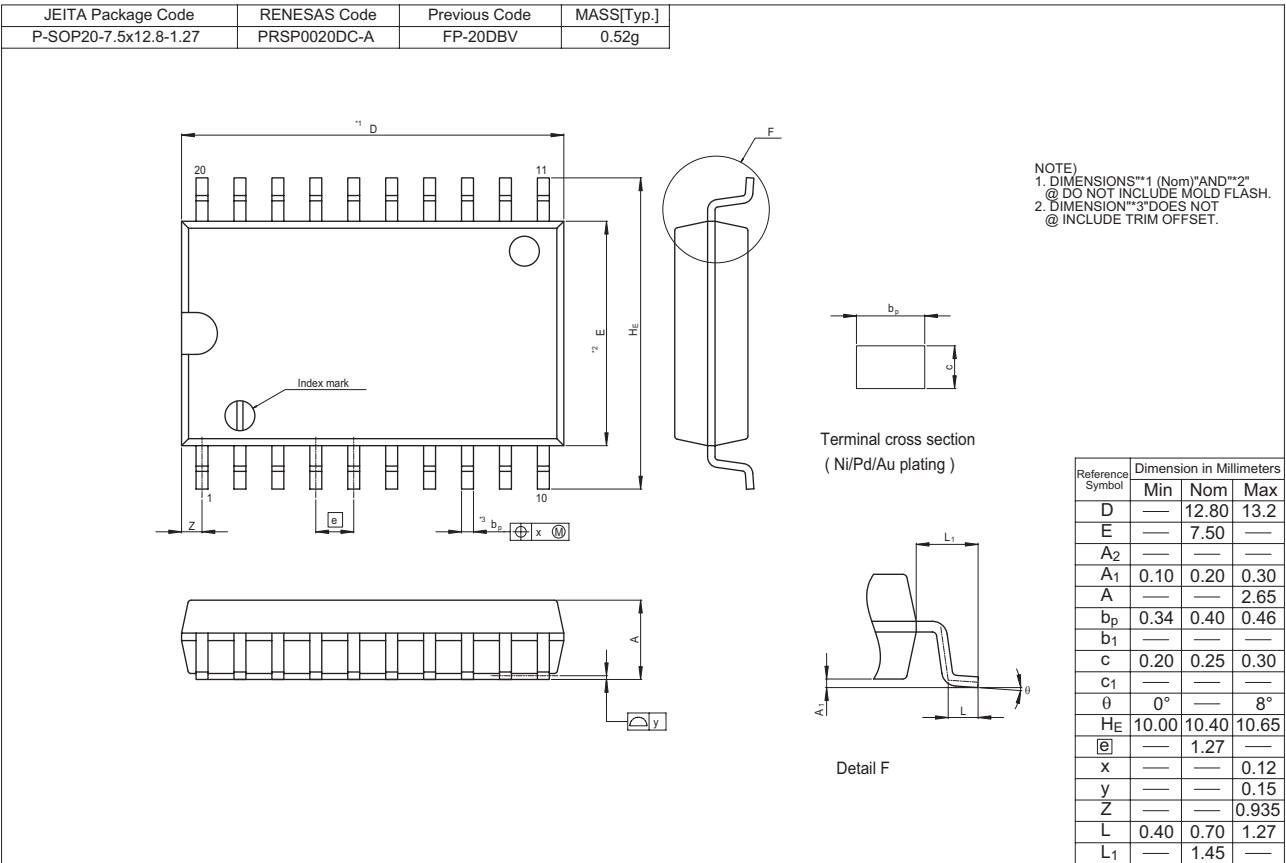
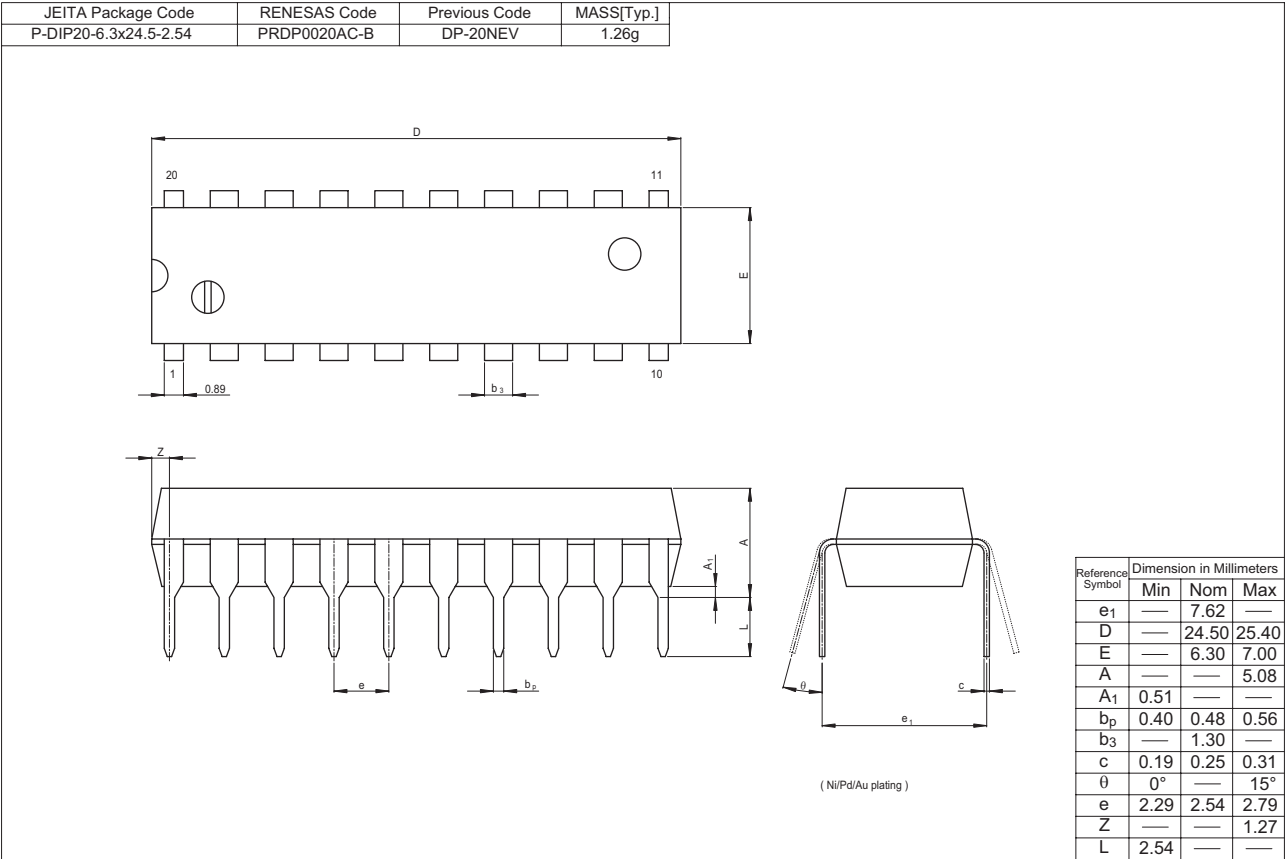


## • Waveform – 2



- Notes :
1. Input waveform :  $PRR \leq 1 \text{ MHz}$ , duty cycle 50%,  $t_r \leq 6 \text{ ns}$ ,  $t_f \leq 6 \text{ ns}$
  2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

Package Dimensions





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