



P-Channel 20-V (D-S) MOSFET

TrenchFET®
MOSFETs
1.5-V Rated



**ESD Protected
2000 V**

PRODUCT SUMMARY		
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (mA)
-20	8 @ V _{GS} = -4.5 V	-150
	12 @ V _{GS} = -2.5 V	-125
	15 @ V _{GS} = -1.8 V	-100
	20 @ V _{GS} = -1.5 V	-30

FEATURES

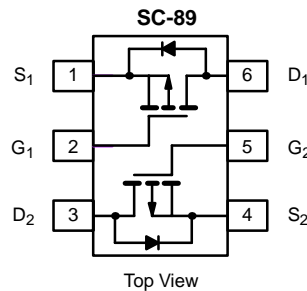
- High-Side Switching
- Low On-Resistance: 8 Ω
- Low Threshold: 0.9 V (typ)
- Fast Switching Speed: 45 ns (typ)
- 1.5-V Operation
- Gate-Source ESD Protection

BENEFITS

- Ease in Driving Switches
- Low Offset (Error) Voltage
- Low-Voltage Operation
- High-Speed Circuits
- Low Battery Voltage Operation

APPLICATIONS

- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits
- Load/Power Switching Cell Phones, Pagers



Marking Code: K

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	5 secs	Steady State	Unit	
Drain-Source Voltage	V _{DS}	-20		V	
Gate-Source Voltage	V _{GS}	±5			
Continuous Drain Current (T _J = 150 °C) ^a	I _D	T _A = 25 °C	-155	-145	mA
		T _A = 85 °C	-110	-105	
Pulsed Drain Current ^b	I _{DM}	-650			
Continuous Source Current (diode conduction) ^a	I _S	-450	-380		
Maximum Power Dissipation ^a	P _D	T _A = 25 °C	280	250	mW
		T _A = 85 °C	145	130	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150		°C	
Gate-Source ESD Rating (HBM, Method 3015)	ESD	2000		V	

Notes

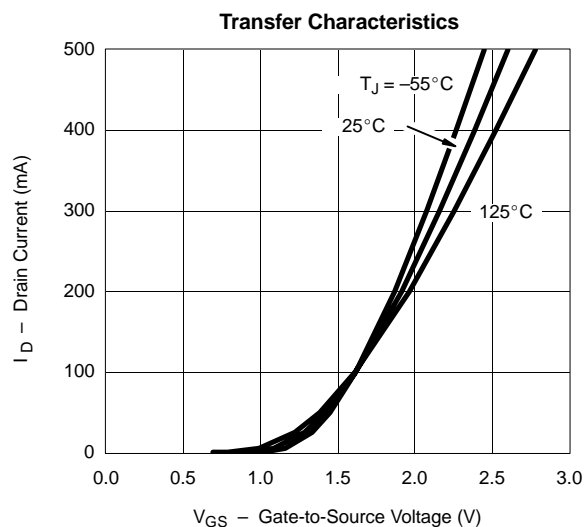
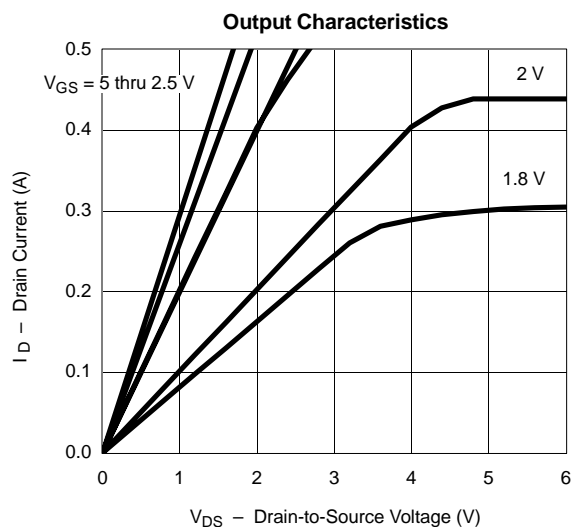
- Surface Mounted on FR4 Board.
- Pulse width limited by maximum junction temperature.

SPECIFICATIONS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.40		-1.20	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 2.8\ \text{V}$		± 0.5	± 1	μA
		$V_{DS} = 0\ \text{V}, V_{GS} = \pm 4.5\ \text{V}$		± 1	± 2	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}$		-1	-500	nA
		$V_{DS} = -16\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 85^\circ\text{C}$			-10	μA
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5\ \text{V}, V_{GS} = -4.5\ \text{V}$	-200			mA
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\ \text{V}, I_D = -150\ \text{mA}$			8	Ω
		$V_{GS} = -2.5\ \text{V}, I_D = -125\ \text{mA}$			12	
		$V_{GS} = -1.8\ \text{V}, I_D = -100\ \text{mA}$			15	
		$V_{GS} = -1.5\ \text{V}, I_D = -30\ \text{mA}$			20	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\ \text{V}, I_D = -150\ \text{mA}$		0.4		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -150\ \text{mA}, V_{GS} = 0\ \text{V}$			-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10\ \text{V}, V_{GS} = -4.5\ \text{V}, I_D = -150\ \text{mA}$		1500		μC
Gate-Source Charge	Q_{gs}			150		
Gate-Drain Charge	Q_{gd}			450		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\ \text{V}, R_L = 65\ \Omega$ $I_D \cong -150\ \text{mA}, V_{GEN} = -4.5\ \text{V}, R_G = 10\ \Omega$			55	ns
Rise Time	t_r				30	
Turn-Off Delay Time	$t_{d(off)}$				60	
Fall Time	t_f				30	

Notes

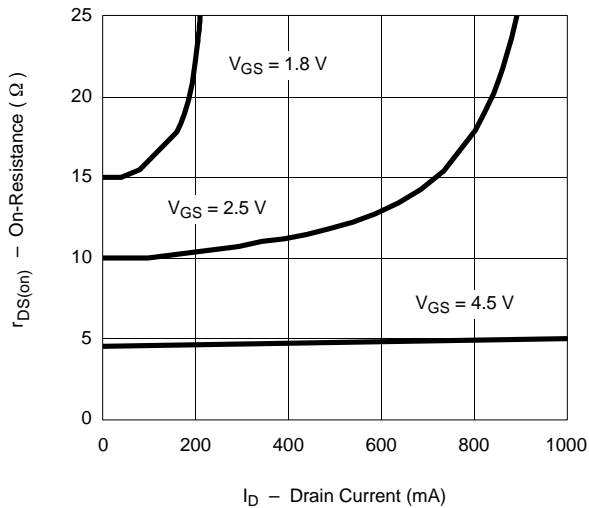
- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ UNLESS NOTED)

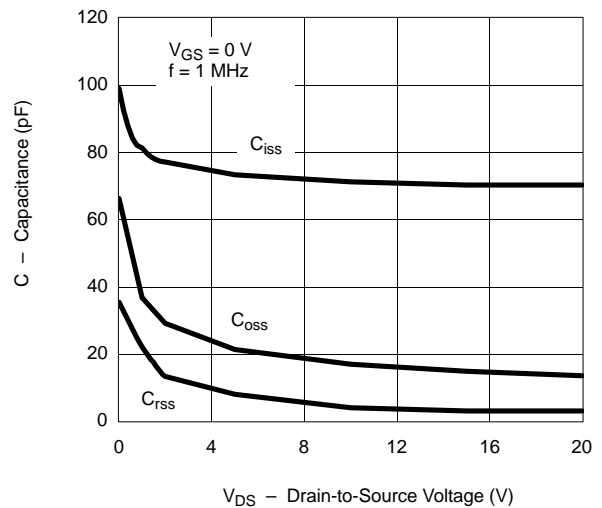


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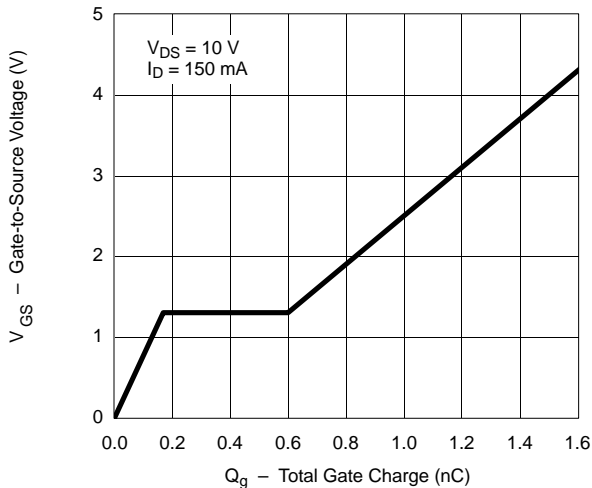
On-Resistance vs. Drain Current



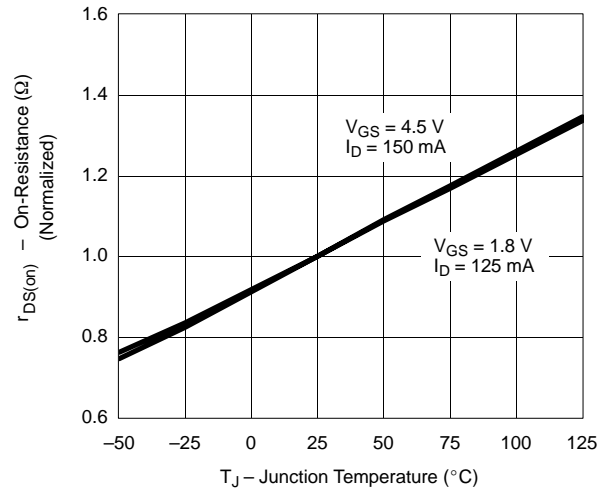
Capacitance



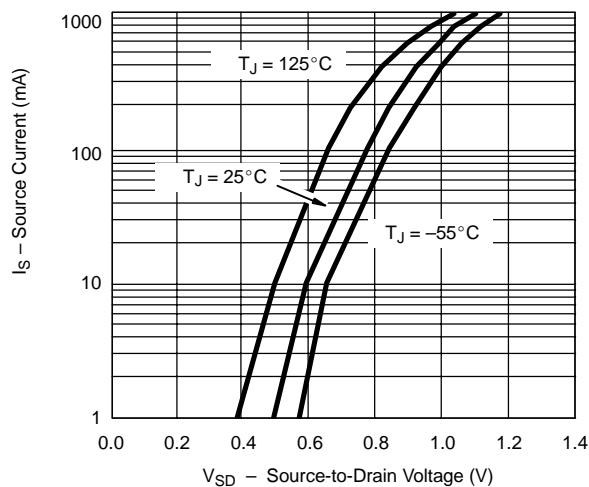
Gate Charge



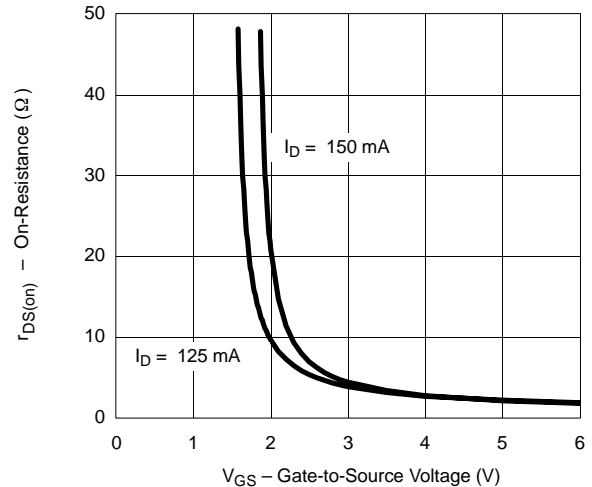
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS NOTED)

