

SERIES REGULATOR WITH RESET FUNCTION

■ GENERAL DESCRIPTION

The NJM78LR05 is a series regulator with reset function.

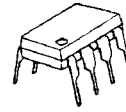
In case of shut down or output voltage drop, the IC generates reset signal to a microcomputer.

That is suitable for items with microcomputer, such as TV sets, remote controller, refrigerator and others.

■ FEATURES

- Output Current  $I_o = 150\text{mA max.}$
- Reset Function Including
- Reset Delay Time can be Adjusted by an External Capacitance.
- Internal Over Current Protection
- Thermal Shut Down
- Bipolar Technology
- Package Outline DIP8, DMP8, SIP8, SOT-89 (5Pin)

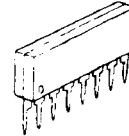
■ PACKAGE OUTLINE



NJM78LR05BD/CD/DD



NJM78LR05BM/CM/DM



NJM78LR05BL/GL/DL



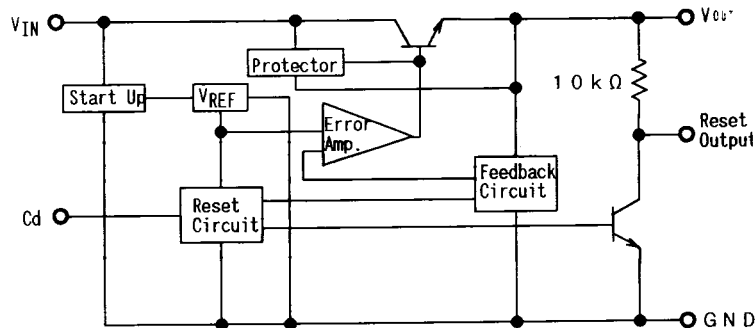
NJM78LR05BU/CU/DU

■ RESET THRESHOLD VOLTAGE LINE-UP

Reset Threshold Voltage	Version	Part Number
4.0V	D	NJM78LR05DX
4.2V	C	NJM78LR05CX
4.3V	B	NJM78LR05DX

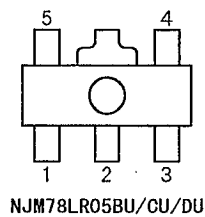
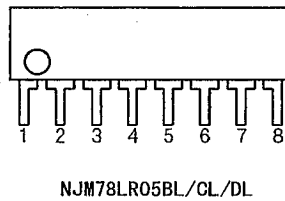
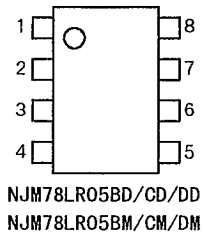
"X" is package suffix.

■ BLOCK DIAGRAM



# NJM78LR05

## PIN CONFIGURATION



### PIN FUNCTION

1. INPUT
2. NC
3. Cd
4. NC
5. GND
6. RESET-OUTPUT
7. NC
8. OUTPUT

### PIN FUNCTION

1. Cd
2. GND
3. RESET-OUTPUT
4. OUTPUT
5. INPUT

## ABSOLUTE MAXIMUM RATINGS

( $T_a = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	MAXIMUM RATINGS	UNIT
Input Voltage	$V_{IN}$	+20	V
Power Dissipation	$P_D$	(DIP8) 500 (DMP8) 500※ (SIP8) 800 (SOT-89) 350	mW
Operating Temperature Range	$T_{opr}$	-40 ~ +85	$^\circ\text{C}$
Storage Temperature Range	$T_{stg}$	-50 ~ +150	$^\circ\text{C}$

※At on PC board.

## RECOMMENDED OPERATING CONDITIONS

( $T_a = 25^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	UNIT
Input Voltage	$V_{IN}$	7.5 ~ 18	V
Output Current	$I_o$	1 ~ 100	mA

6

■ ELECTRICAL CHARACTERISTICS ( $V_{IN}=10V$ ,  $I_o=40mA$ ,  $C_{IN}=1\mu F$ ,  $C_o=10\mu F$ ,  $T_a=25^\circ C$ )  
 [Power Supply Block]

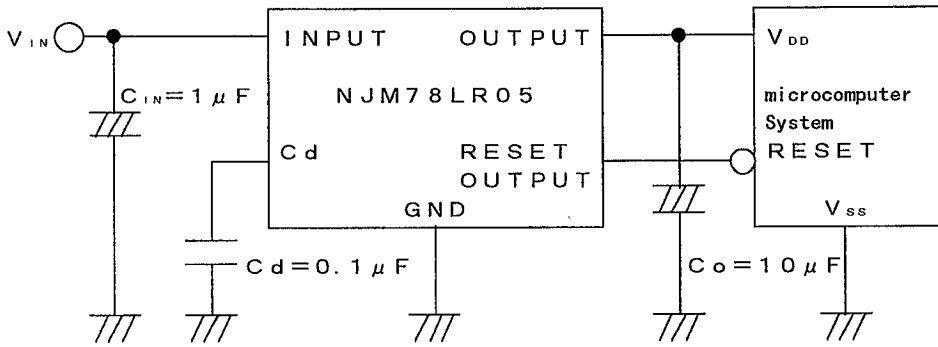
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	$V_o$	$I_o=1mA$	4.80	5.00	5.20	V
Quiescent Current	$I_q$	$I_o=100mA$	—	1.40	3.40	mA
Output Short Current	$I_{osc}$	OUTPUT-GND short	150	300	450	mA
Line Regulation 1	$\Delta V_o/V_{IN1}$	$7V \leq V_{IN} \leq 18V$	—	6.0	65.0	mV
Line Regulation 2	$\Delta V_o/V_{IN2}$	$8V \leq V_{IN} \leq 18V$	—	3.0	42.0	mV
Load Regulation 1	$\Delta V_o/I_{o1}$	$I_o=1 \sim 100mA$	—	9.0	60.0	mV
Load Regulation 2	$\Delta V_o/I_{o2}$	$I_o=1 \sim 40mA$	—	3.0	30.0	mV
Ripple Rejection	RR	$f=120Hz$ , $e_{i,rms}=1V_{p-p}$ , $V_{IN}=8 \sim 18V$	—	79	—	dB
Output Noise Voltage	$V_{no}$	$10Hz \leq f \leq 100kHz$ , $I_o=1mA$	—	80	—	$\mu V$
Dropout Voltage	$\Delta V_{I-o}$		—	1.5	2.2	V

[Reset Block]

(H) Reset Output Voltage	$V_{ORH}$		4.80	5.00	5.20	V
(L) Reset Output Voltage	$V_{ORL}$	$V_{IN}=3V$ , $I_o=1mA$	—	10	200	mV
Reset Threshold Voltage	$V_{RT}$	B Version	4.12	4.30	4.48	V
		C Version	4.03	4.20	4.37	
		D Version	3.84	4.00	4.16	
Reset Threshold Hysteresis Voltage	$V_{RTH}$		50	100	200	mV
Reset Output Delay Time	$t_d$	$C_d=0.1\mu F$	7.50	10.0	12.5	ms

# NJM78LR05

## APPLICATION CIRCUIT

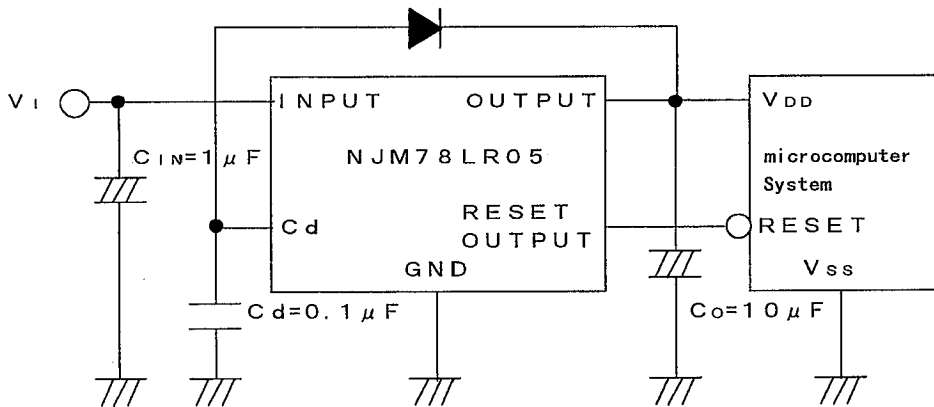


$$t_d [\text{ms}] = 100 \times C_d [\mu\text{F}]$$

Note1: When the capacitance  $C_d$  is too large, the actual delay time is shorter than the calculated result because an electrical charge of  $C_d$  is discharged incompletely.

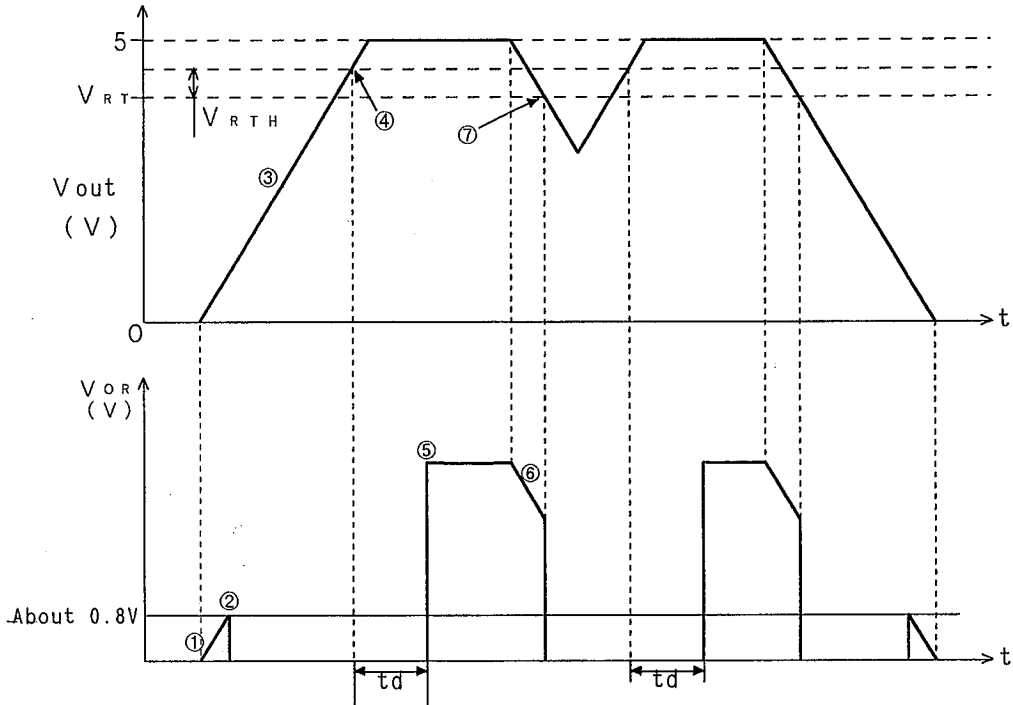
Solution of above problem:

- (1) Connect SBD between output terminal and  $C_d$  terminal. Please refer to the following circuit.
- (2) Select larger capacitance,  $C_{IN}$  than  $C_d$ .



6

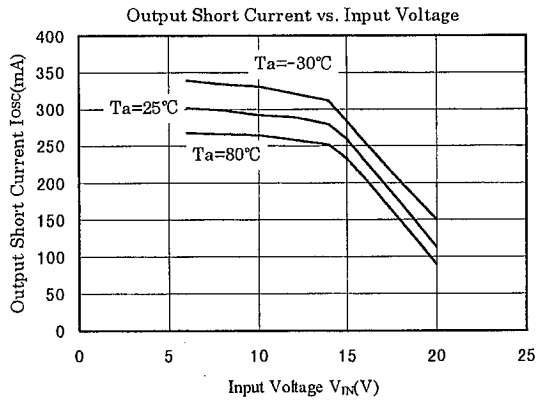
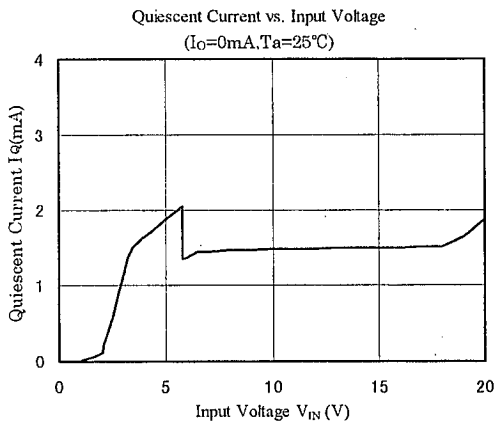
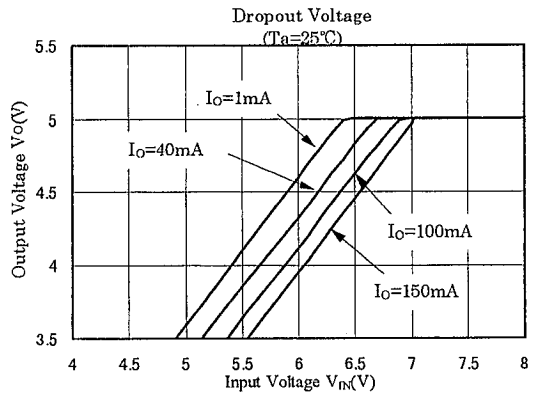
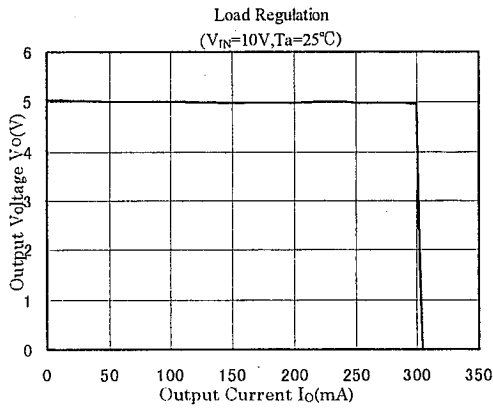
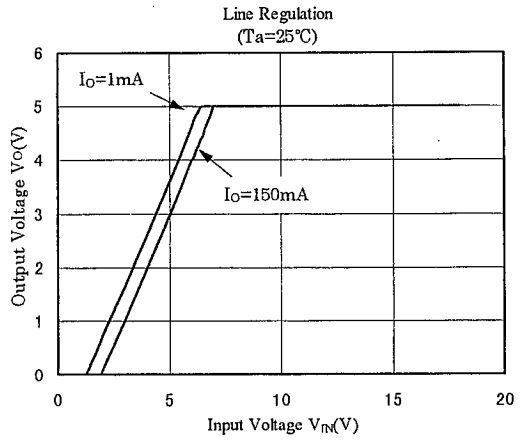
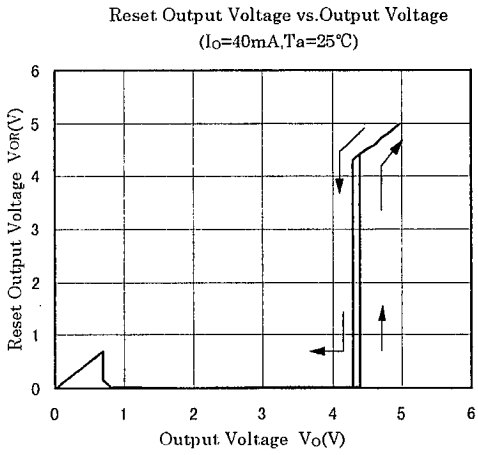
■ TIMING CHART



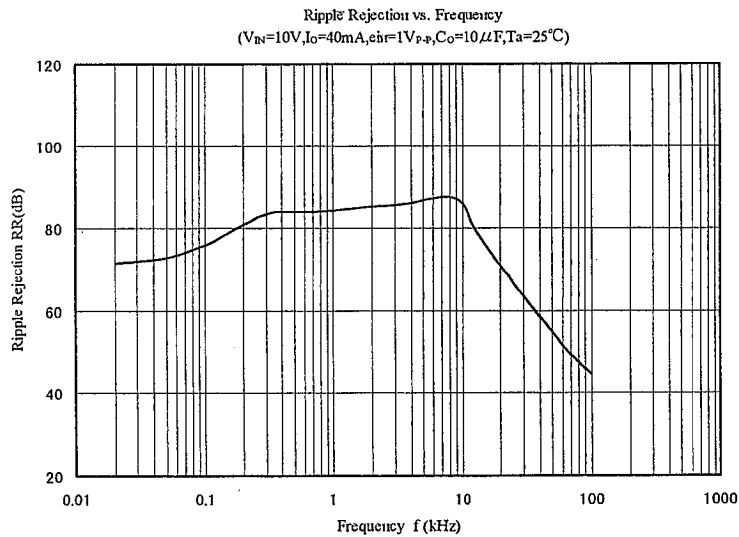
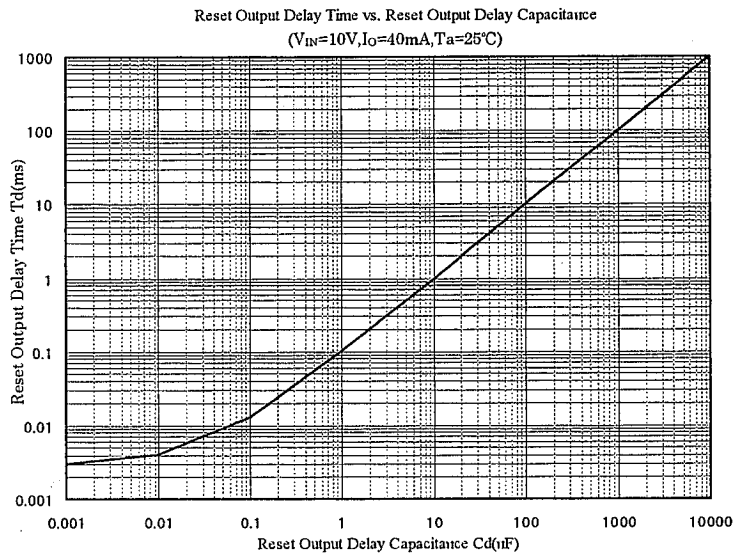
- ① When the input voltage is up to about 0.8V, some voltage is outputted at the reset output because the NJM78LR05 operation is unstable.
- ② When the input voltage goes over about 0.8V, the reset output becomes "L".
- ③ The output voltage is rising up with the input voltage.
- ④ When the output voltage goes over  $(V_{RT} + V_{RTH})$ , the delay circuit of reset output activates.  
 $V_{RT}$ : Reset Threshold Voltage  
 $V_{RTH}$ : Reset Threshold Hysteresis Voltage
- ⑤ After the reset output delay time  $t_d$  has passed, the reset output becomes "H".
- ⑥ The output voltage is falling down with the input voltage.
- ⑦ When the output voltage is less than  $V_{RT}$ , the reset output becomes "L".

6

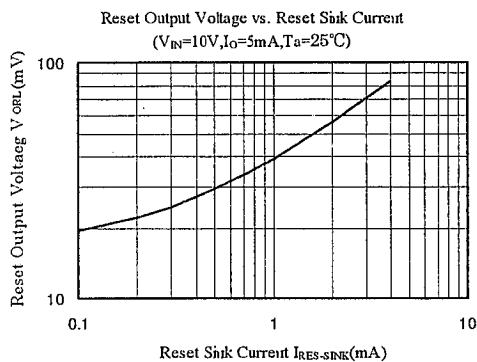
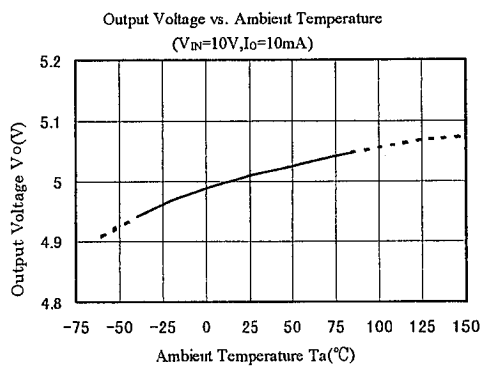
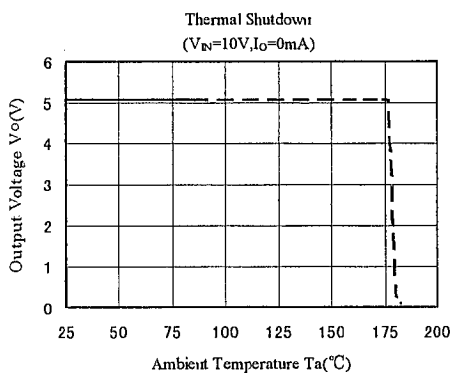
## TYPICAL CHARACTERISTICS



## ■ TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS





---

# MEMO

**[CAUTION]**

The specifications on this databook are only given for information, without any guarantee as regards either mistakes or omissions. The application circuits in this databook are described only to show representative usages of the product and not intended for the guarantee or permission of any right including the industrial rights.