MMBF170LT1, MVBF170LT1

Power MOSFET
500 mA, 60 V
N−Channel SOT−23

Features

- AEC Q101 Qualified − MVBF170LT1
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	60	Vdc
Drain−Gate Voltage	V_{DGS}	60	Vdc
Gate−Source Voltage − Continuous − Non−repetitive ($t_p \le 50$ μs)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current − Continuous − Pulsed	I_D I_{DM}	0.5 0.8	Adc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board (Note 1.) T_A = 25°C Derate above 25°C	P_D	 225 1.8	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	556	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−5 = 1.0 × 0.75 × 0.062 in.

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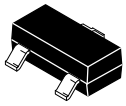
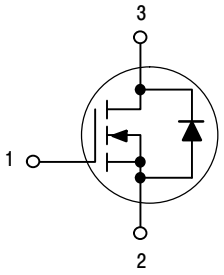
500 mA, 60 V
$R_{DS(on)}$ = 5 Ω

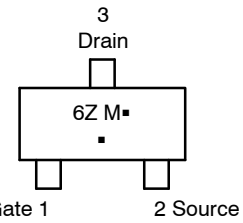


SOT−23
CASE 318
STYLE 21

N−Channel



MARKING DIAGRAM & PIN ASSIGNMENT



6Z = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain−Source Breakdown Voltage (V_{GS} = 0, I_D = 100 μA)		$V_{(BR)DSS}$	60	–	Vdc
Gate−Body Leakage Current, Forward (V_{GSF} = 15 Vdc, V_{DS} = 0)		I_{GSS}	–	10	nAdc
ON CHARACTERISTICS (Note 1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	0.8	3.0	Vdc
Static Drain−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 200 mA)		$r_{DS(on)}$	–	5.0	Ω
On−State Drain Current (V_{DS} = 25 Vdc, V_{GS} = 0)		$I_{D(off)}$	–	0.5	μA
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 10 Vdc, V_{GS} = 0 V, f = 1.0 MHz)		C_{iss}	–	60	pF
SWITCHING CHARACTERISTICS (Note 1)					
Turn−On Delay Time	(V_{DD} = 25 Vdc, I_D = 500 mA, R_{gen} = 50 Ω) Figure 1	$t_{d(on)}$	–	10	ns
Turn−Off Delay Time		$t_{d(off)}$	–	10	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

ORDERING INFORMATION

Device	Package	Shipping†
MMBF170LT1G	SOT−23 (TO−236) (Pb−Free)	3000 / Tape & Reel
MMBF170LT3G	SOT−23 (TO−236) (Pb−Free)	10000 / Tape & Reel
MVBF170LT1G	SOT−23 (TO−236) (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

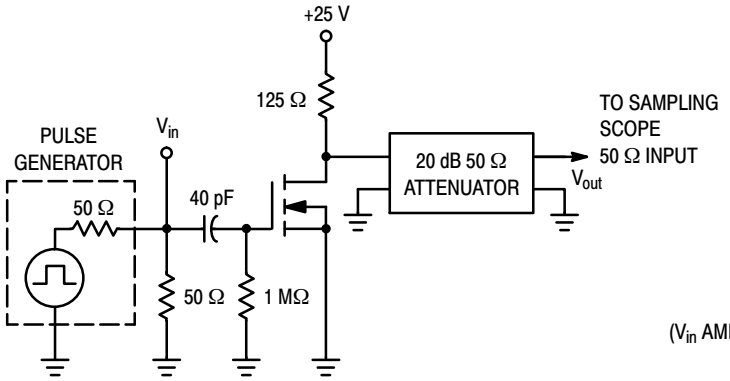


Figure 1. Switching Test Circuit

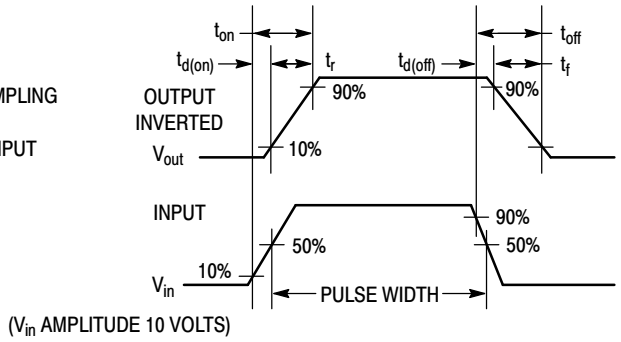


Figure 2. Switching Waveform

TYPICAL ELECTRICAL CHARACTERISTICS

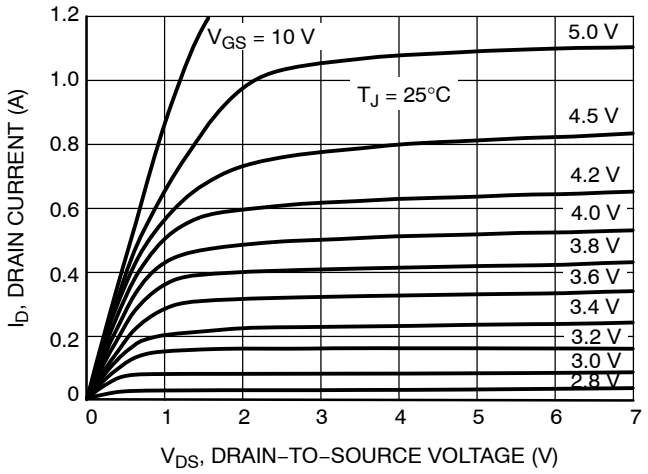


Figure 3. On−Region Characteristics

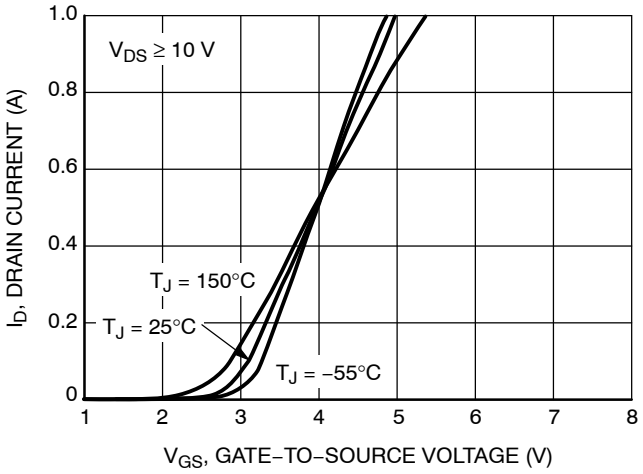


Figure 4. Transfer Characteristics

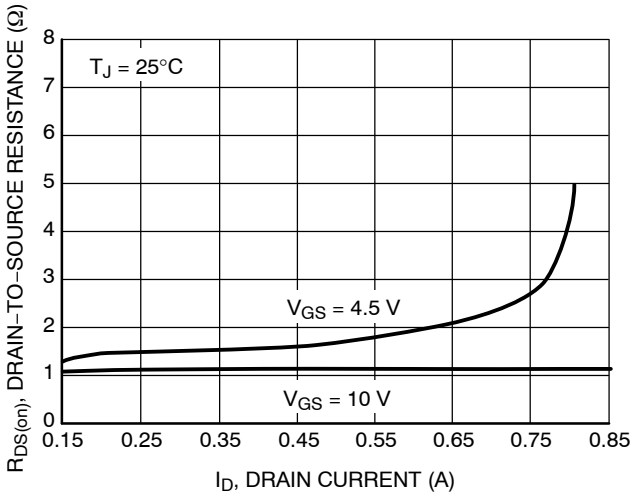


Figure 5. On−Resistance vs. Drain Current and Gate Voltage

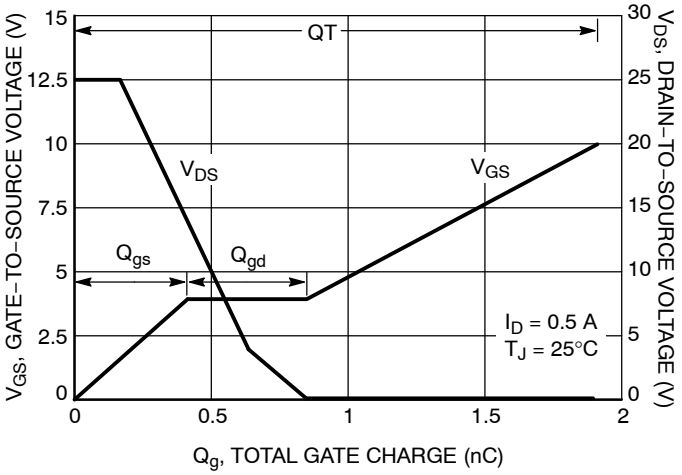


Figure 6. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

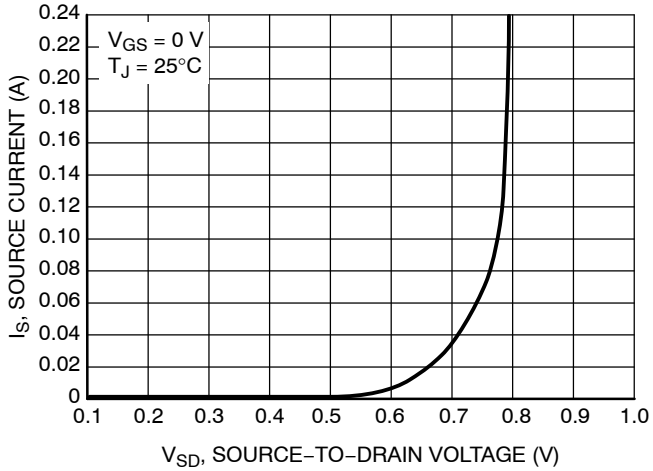


Figure 7. Diode Forward Voltage vs. Current

TYPICAL ELECTRICAL CHARACTERISTICS

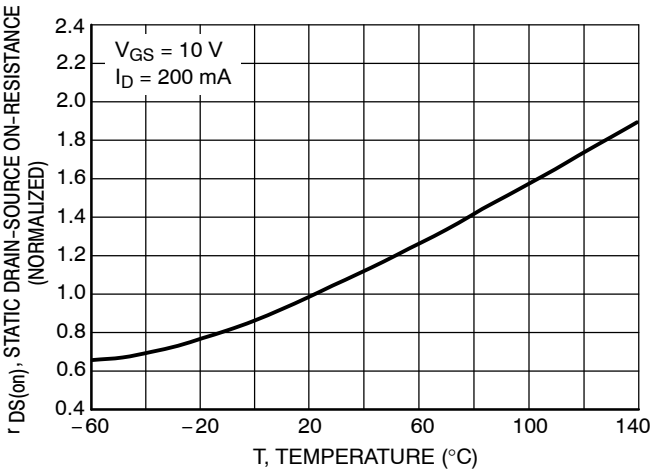


Figure 8. Temperature versus Static Drain−Source On−Resistance

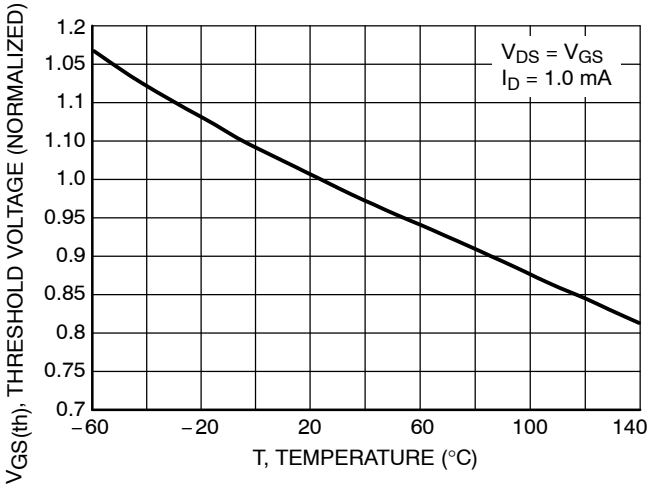
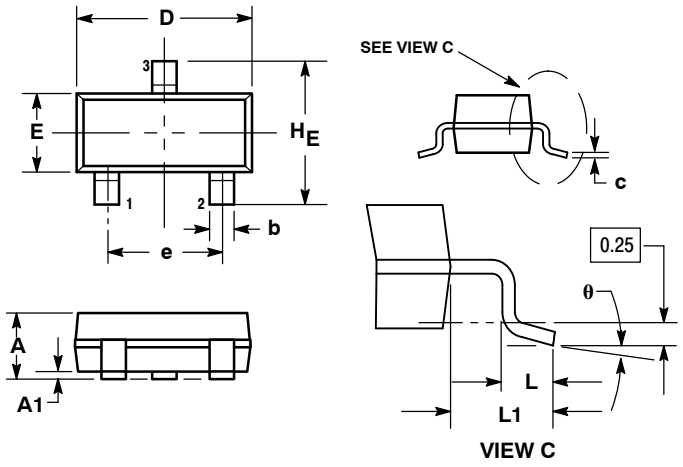


Figure 9. Temperature versus Gate Threshold Voltage

PACKAGE DIMENSIONS

SOT−23 (TO−236)
CASE 318−08
ISSUE AP

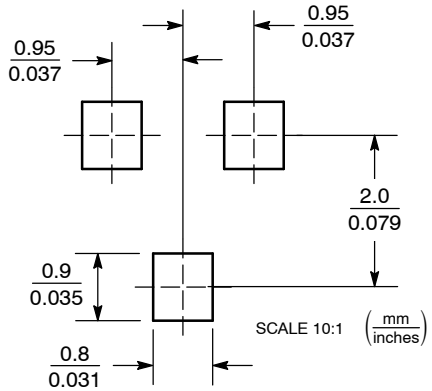


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.40	2.64	0.083	0.094	0.104
θ	0°	−−−	10°	0°	−−−	10°

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

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