

2SK3289

Silicon N Channel MOS FET
High Speed Switching

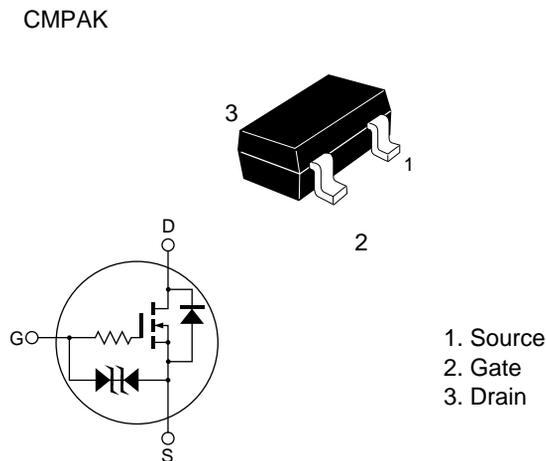
HITACHI

ADE-208-743B(Z)
Target Specification 3rd.Edition.
December 1998

Features

- Low on-resistance
 $R_{DS} = 1.26\Omega$ typ. (at $V_{GS} = 10V$, $I_D = 150mA$)
 $R_{DS} = 2.8\Omega$ typ. (at $V_{GS} = 4V$, $I_D = 50mA$)
- 4V gate drive device
- Small package (CMPAK)

Outline



Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	300	mA
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	1.2	A
Body-drain diode reverse drain current	I_{DR}	300	mA
Channel dissipation	Pch ^{Note 2}	400	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

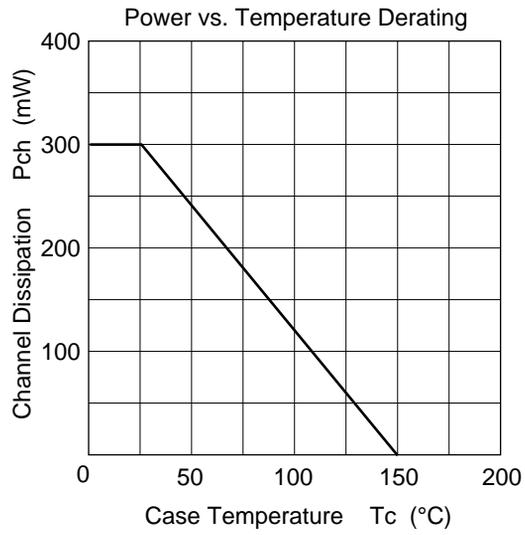
Note: 1. PW ≤ 10μs, duty cycle ≤ 1 %
 2. Value on the alumina ceramic board (12.5x20x0.7mm)

Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 100\mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100\mu A, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±5	μA	$V_{GS} = \pm 16V, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.3	—	2.3	V	$I_D = 10\mu A, V_{DS} = 5V$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.26	1.44	Ω	$I_D = 150mA, V_{GS} = 10V$ ^{Note 3}
	$R_{DS(on)}$	—	2.8	3.44	Ω	$I_D = 50mA, V_{GS} = 4V$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	145	220	—	mS	$I_D = 150mA, V_{DS} = 10V$ ^{Note 3}
Input capacitance	Ciss	—	4	—	pF	$V_{DS} = 10V$
Output capacitance	Coss	—	15	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	2	—	pF	f = 1MHz
Turn-on delay time	$t_{d(on)}$	—	200	—	ns	$I_D = 150mA, V_{GS} = 10V$
Rise time	t_r	—	600	—	ns	$R_L = 66.6\Omega$
Turn-off delay time	$t_{d(off)}$	—	1100	—	ns	
Fall time	t_f	—	1100	—	ns	

Note: 3. Pulse test
 4. Marking is "AN"

Main Characteristics



Cautions

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