

# 2SK3349

Silicon N Channel MOS FET  
High Speed Switching

# HITACHI

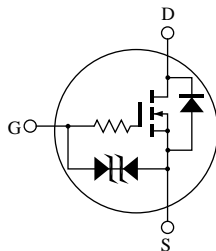
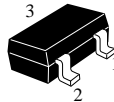
ADE-208-804 (Z)  
1st.Edition.  
June 1999

## Features

- Low on-resistance  
 $R_{DS} = 2.8$  typ. (at  $V_{GS} = 4$  V ,  $I_D = 25$  mA)  
 $R_{DS} = 4.8$  typ. (at  $V_{GS} = 2.5$  V ,  $I_D = 10$  mA)
- 2.5 V gate drive device
- Small package (SMPAK)

## Outline

SMPAK



1. Source
2. Gate
3. Drain

## Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	20	V
Gate to source voltage	$V_{GSS}$	±10	V
Drain current	$I_D$	50	mA
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	200	mA
Body-drain diode reverse drain current	$I_{DR}$	50	mA
Channel dissipation	$P_{ch}$ <sup>Note 2</sup>	100	mW
Channel temperature	$T_{ch}$	150	°C
Storage temperature	$T_{stg}$	-55 to +150	°C

Note: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. Value on the alumina ceramic board (12.5x20x0.7 mm)

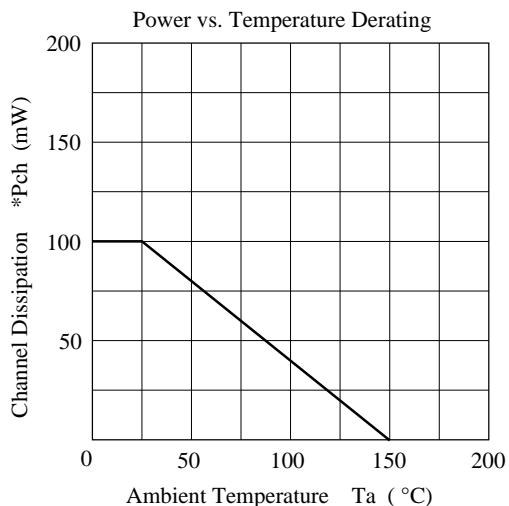
## Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	20	—	—	V	$I_D = 100 \mu A, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±10	—	—	V	$I_G = \pm 100 \mu A, V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±5	μA	$V_{GS} = \pm 8 V, V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	μA	$V_{DS} = 20 V, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	0.8	—	1.8	V	$I_D = 10 \mu A, V_{DS} = 5 V$
Static drain to source on state resistance	$R_{DS(on)}$	—	2.8	3.6	Ω	$I_D = 25 mA, V_{GS} = 4 V$ <sup>Note 3</sup>
	$R_{DS(on)}$	—	4.8	7.2	Ω	$I_D = 10 mA, V_{GS} = 2.5 V$ <sup>Note 3</sup>
Forward transfer admittance	$ y_{fs} $	56	85	—	mS	$I_D = 25 mA, V_{DS} = 10 V$ <sup>Note 3</sup>
Input capacitance	$C_{iss}$	—	6	—	pF	$V_{DS} = 10 V$
Output capacitance	$C_{oss}$	—	7	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	1.2	—	pF	$f = 1 MHz$
Turn-on delay time	$t_{d(on)}$	—	120	—	ns	$I_D = 25 mA, V_{GS} = 4 V$
Rise time	$t_r$	—	450	—	ns	$R_L = 400 \Omega$
Turn-off delay time	$t_{d(off)}$	—	480	—	ns	
Fall time	$t_f$	—	500	—	ns	

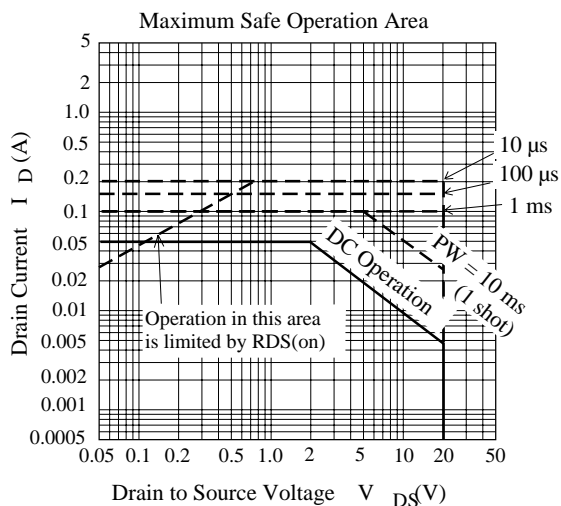
Note: 3. Pulse test

4. Marking is DN

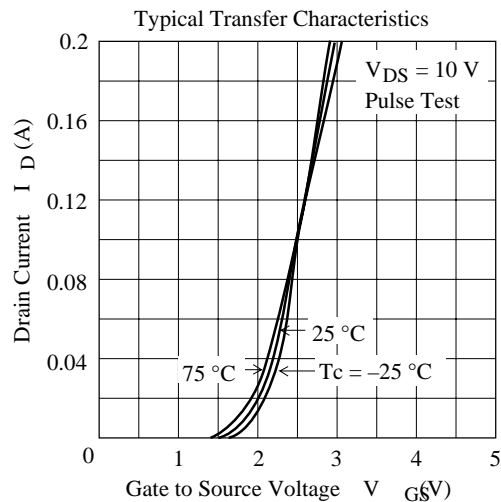
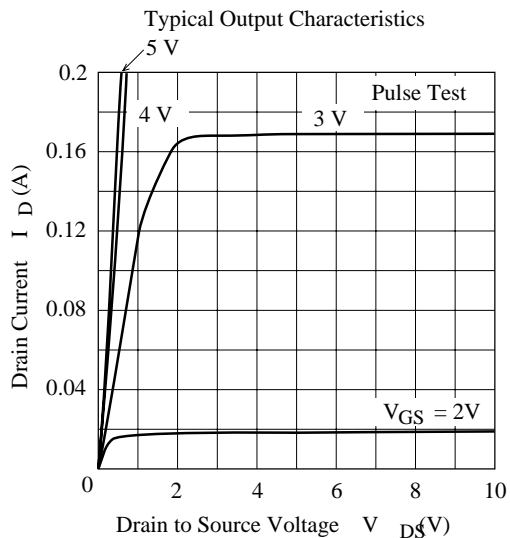
## Main Characteristics



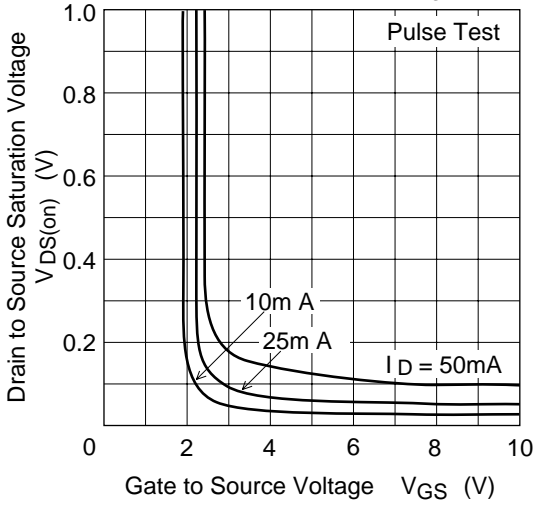
\*Value on the alumina ceramic board.(12.5x20x0.7mm)



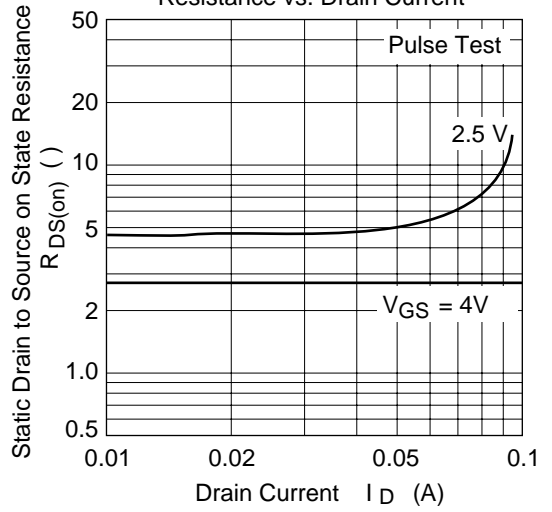
Value on the alumina ceramic board.(12.5x20x0.7mm)



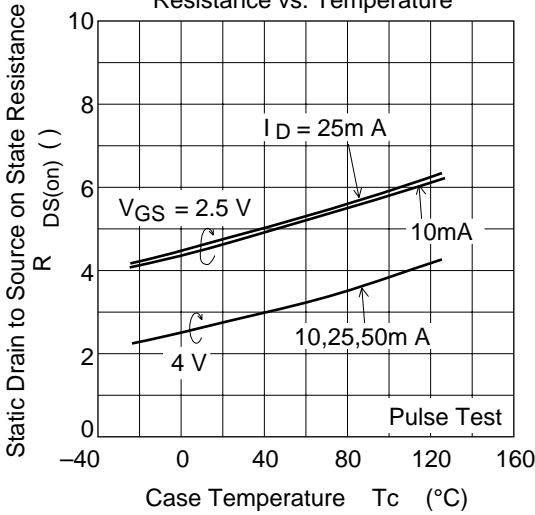
Drain to Source Saturation Voltage vs. Gate to Source Voltage



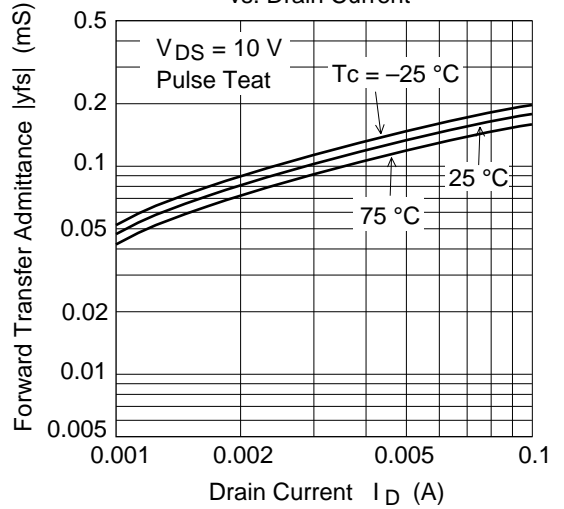
Static Drain to Source on State Resistance vs. Drain Current

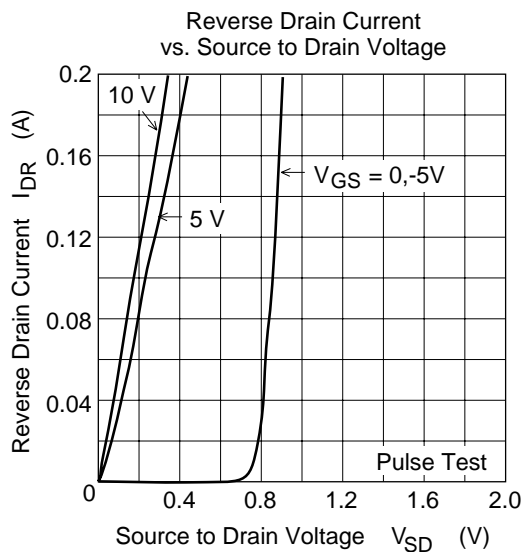
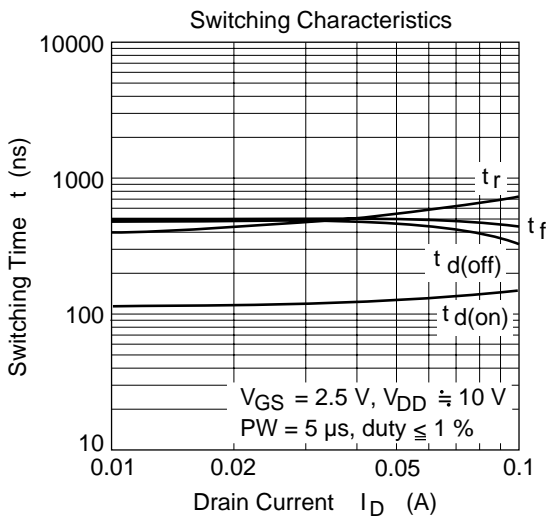
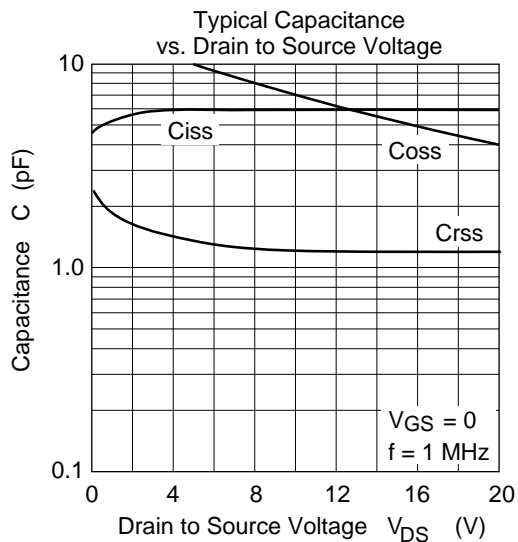


Static Drain to Source on State Resistance vs. Temperature

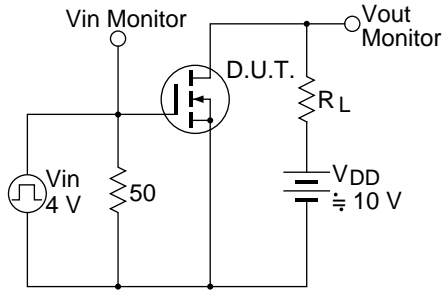


Forward Transfer Admittance vs. Drain Current

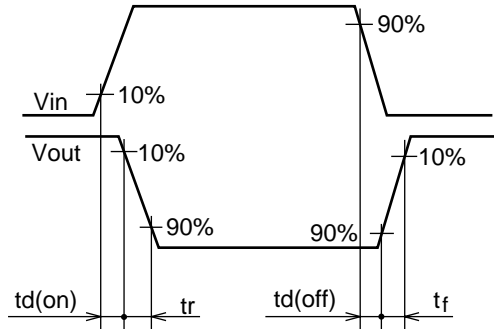




Switching Time Test Circuit



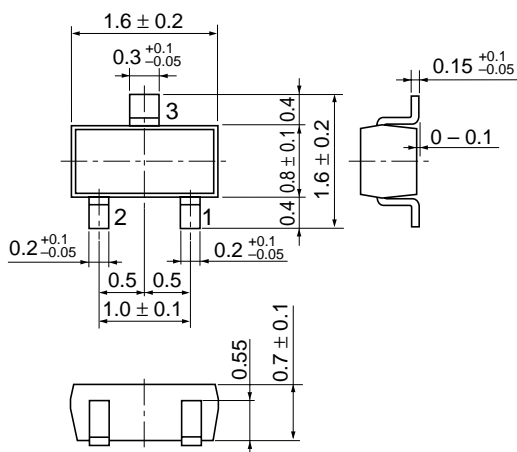
Waveforms



## Package Dimensions

As of January, 2001

Unit: mm



Hitachi Code	SMPAK
JEDEC	—
EIAJ	Conforms
Mass (reference value)	0.003 g

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