

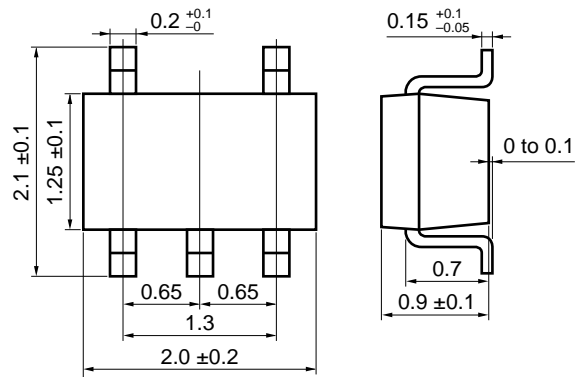
N-CHANNEL MOS FET (5-PIN 2 CIRCUITS)  
 FOR SWITCHING

The  $\mu$ PA572T is a super-mini-mold device provided with two MOS FET circuits. It achieves high-density mounting and saves mounting costs.

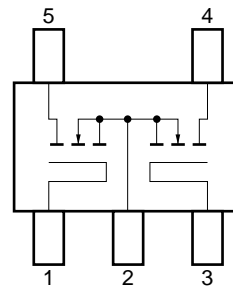
FEATURES

- Two source common MOS FET circuits in package the same size as SC-70
- Directly driven by 3 V power supply
- Automatic mounting supported

PACKAGE DIMENSIONS (in millimeters)



EQUIVALENT CIRCUIT



PIN CONNECTION

1. Gate 1 (G1)
  2. Source (common)
  3. Gate 2 (G2)
  4. Drain 2 (D2)
  5. Drain 1 (D1)
- Marking: DB

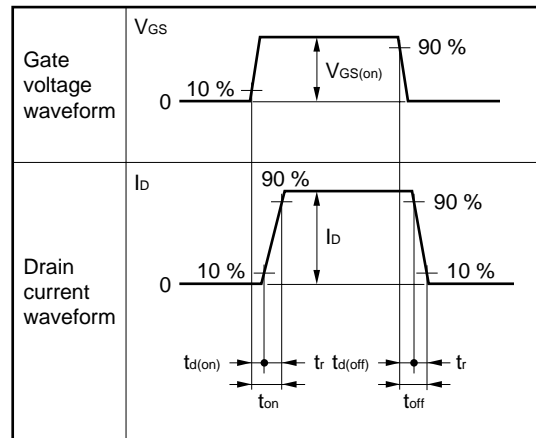
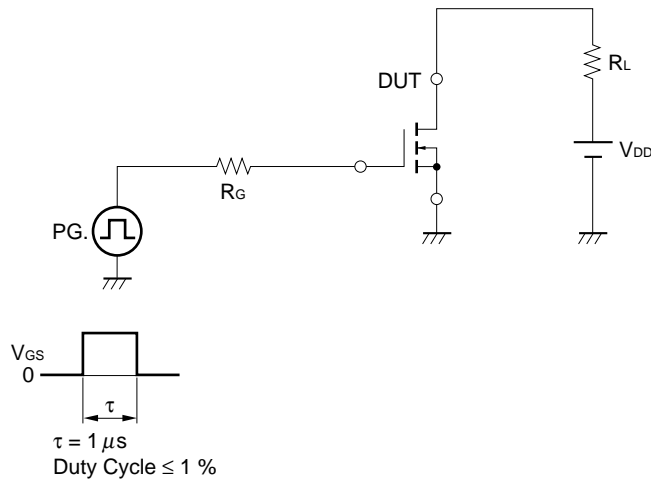
ABSOLUTE MAXIMUM RATINGS ( $T_A = 25\text{ }^\circ\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Drain to Source Voltage	$V_{DSS}$	$V_{GS} = 0$	30	V
Gate to Source Voltage	$V_{GSS}$	$V_{DS} = 0$	$\pm 7$	V
Drain Current (DC)	$I_{D(DC)}$		$\pm 100$	mA
Drain Current (pulse)	$I_{D(pulse)}$	$PW \leq 10\text{ ms}$ , Duty Cycle $\leq 50\%$	$\pm 200$	mA
Total Power Dissipation	$P_T$		200 (Total)	mW
Channel Temperature	$T_{ch}$		150	$^\circ\text{C}$
Operating Temperature	$T_{opt}$		-55 to +80	$^\circ\text{C}$
Storage Temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS (Ta = 25 °C)**

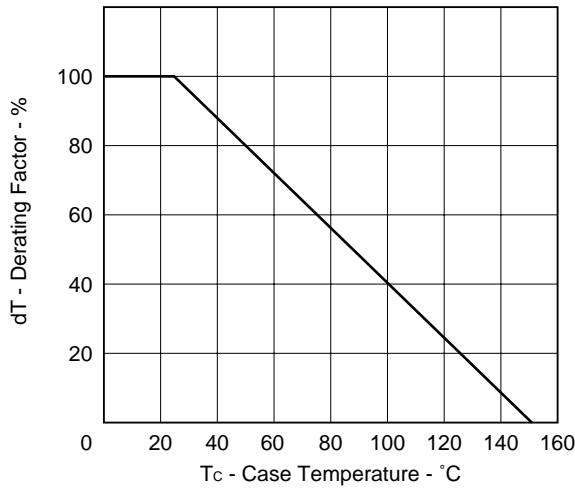
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain Cut-off Current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0$			1.0	$\mu\text{A}$
Gate Leakage Current	$I_{GSS}$	$V_{GS} = \pm 5\text{ V}, V_{DS} = 0$			$\pm 3.0$	$\mu\text{A}$
Gate Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = 3\text{ V}, I_D = 10\ \mu\text{A}$	0.8	1.0	1.5	V
Forward Transfer Admittance	$ y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	20	50		mS
Drain to Source On-State Resistance	$R_{DS(on)1}$	$V_{GS} = 2.5\text{ V}, I_D = 1\text{ mA}$		7	13	$\Omega$
Drain to Source On-State Resistance	$R_{DS(on)2}$	$V_{GS} = 4.0\text{ V}, I_D = 10\text{ mA}$		5	8	$\Omega$
Input Capacitance	$C_{iss}$	$V_{DS} = 5.0\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$		16		pF
Output Capacitance	$C_{oss}$			14		pF
Reverse Transfer Capacitance	$C_{rss}$			2		pF
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 5\text{ V}, I_D = 10\text{ mA}, V_{GS(on)} = 5\text{ V}, R_G = 10\ \Omega, R_L = 500\ \Omega$		15		ns
Rise Time	$t_r$			20		ns
Turn-Off Delay Time	$t_{d(off)}$			100		ns
Fall Time	$t_f$			100		ns

**SWITCHING TIME MEASUREMENT CIRCUIT AND CONDITIONS (RESISTANCE LOADED)**

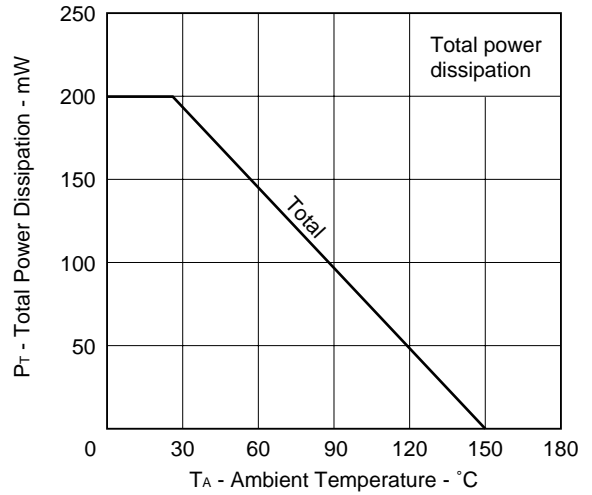


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

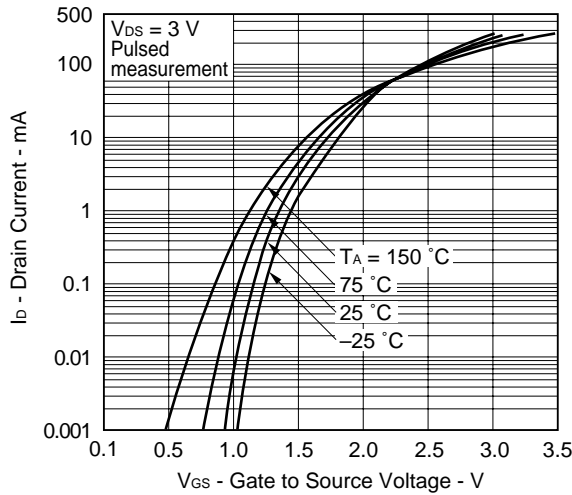
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



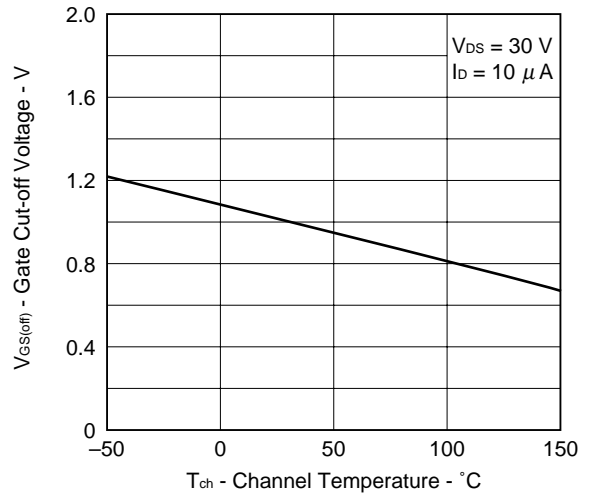
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



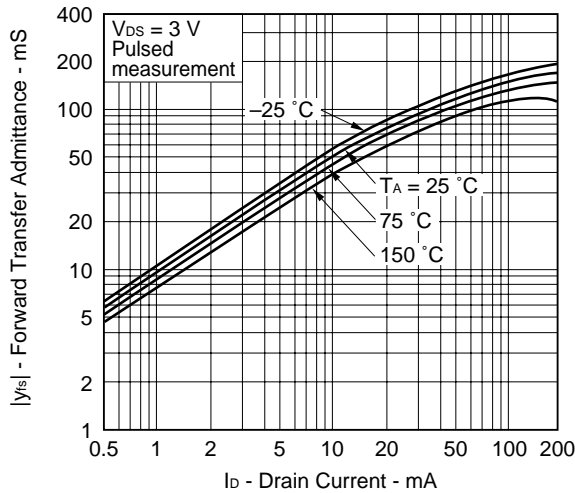
TRANSFER CHARACTERISTICS



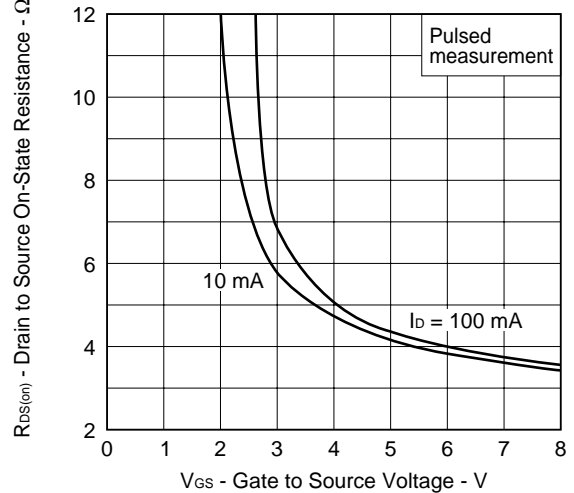
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



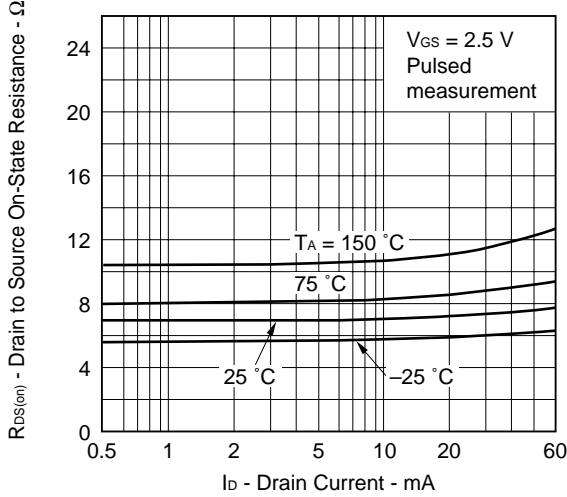
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



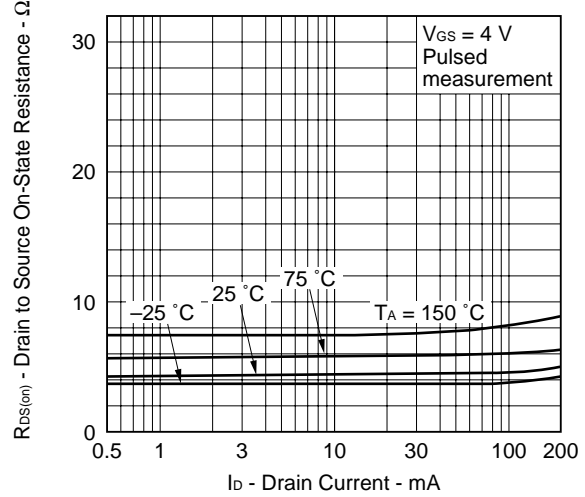
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



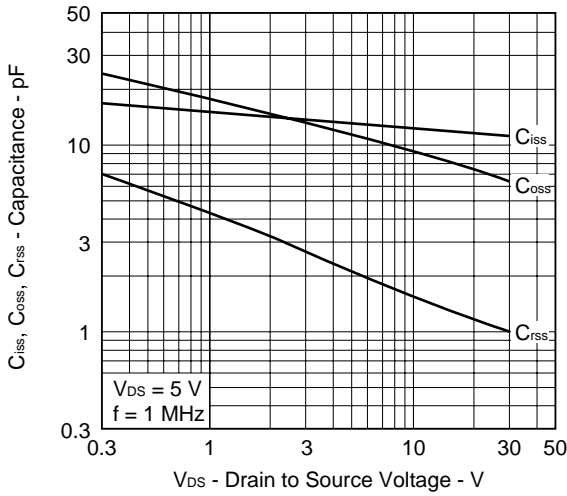
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



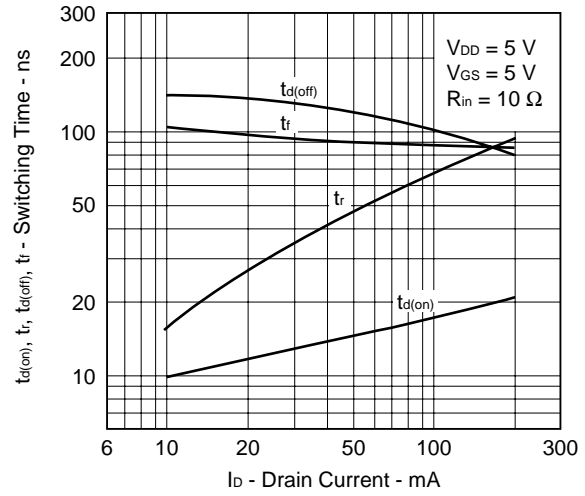
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



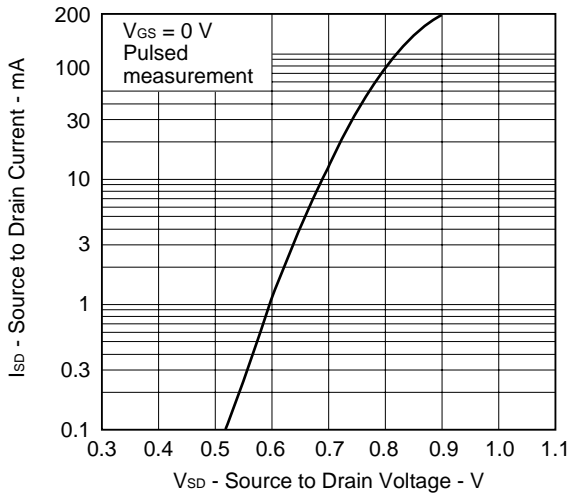
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



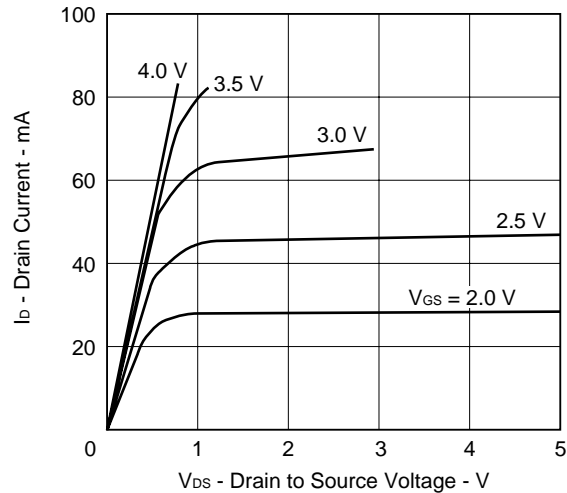
SWITCHING CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



## REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system	TEI-1202
Quality grade on NEC semiconductor devices	IEI-1209
Semiconductor device mounting technology manual	C10535E
Guide to quality assurance for semiconductor devices	MEI-1202
Semiconductor selection guide	X10679E

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Anti-radioactive design is not implemented in this product.