

N-Channel Enhancement Mode MOSFET

GENERAL DESCRIPTION

The ME2306 is the N-Channel logic enhancement mode power field effect transistors, using high cell density, DMOS trench technology.

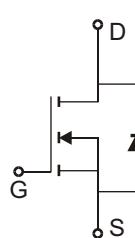
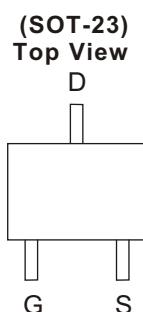
This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone, notebook computer power management and other battery powered circuits, and low in-line power loss that are needed in a very small outline surface mount package.

FEATURES

1. 30V/4A, $R_{DS(ON)}=37m\Omega$ @ $V_{GS}=10V$
2. 30V/3.5A, $R_{DS(ON)}=49m\Omega$ @ $V_{GS}=4.5V$
3. Super high density cell design for extremely low $R_{DS(ON)}$
4. Exceptional on-resistance and maximum DC current capability

PIN CONFIGURATION (SOT-23)



PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

Absolute Maximum Ratings (TA=25°C Unless Otherwise Noted)

Parameter	Symbol	5 secs	Steady State	Units
Drain-Source Voltage	V_{DS}		30	V
Gate-Source Voltage	V_{GS}		± 20	V
Continuous Drain Current($T_J=150^{\circ}C$) ^{a,b}	I_D	4.0	3.16	A
		3.5	2.7	
Pulsed Drain Current	I_{DM}		20	A
Continuous Source Current (Diode Conduction) ^{a,b}	I_S	1.04	0.62	A
Power Dissipation ^{a,b}	P_D	1.25	0.75	W
		0.8	0.48	
Operating Junction Temperature	T_J	-55 to 150		°C

Thermal Resistance Ratings

Parameter	Symbol	Limits		Units
		Typ	Max	
Maximum Junction-to-Ambient ^a	R_{thJA}	80	100	°C/W
		130	166	
Maximum Junction-to-Foot(Drain) Steady-State	R_{thJF}	60	75	°C/W

Notes

a. Surface Mounted on FR4 Board, $t \leq 5$ sec.

b. Pulse width limited by maximum junction temperature.

Electrical Characteristics ($T_J = 25^\circ\text{C}$ Unless Specified)

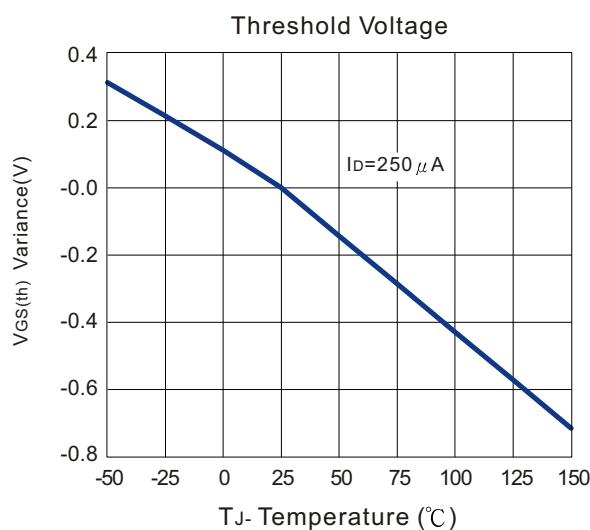
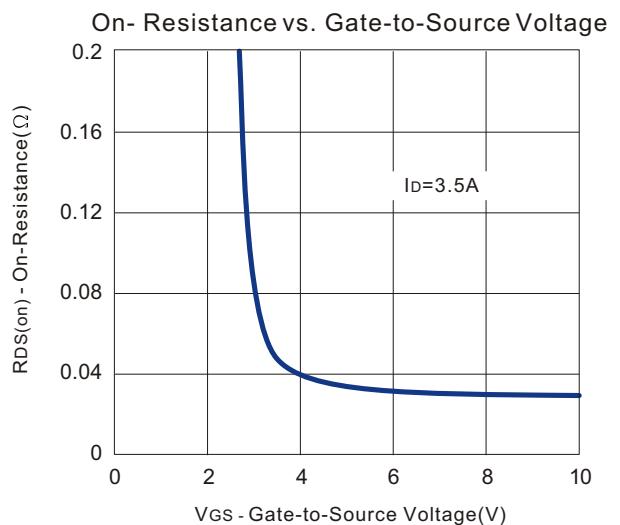
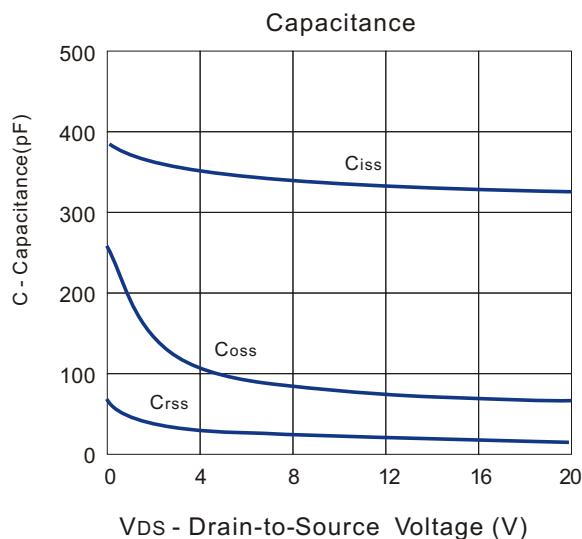
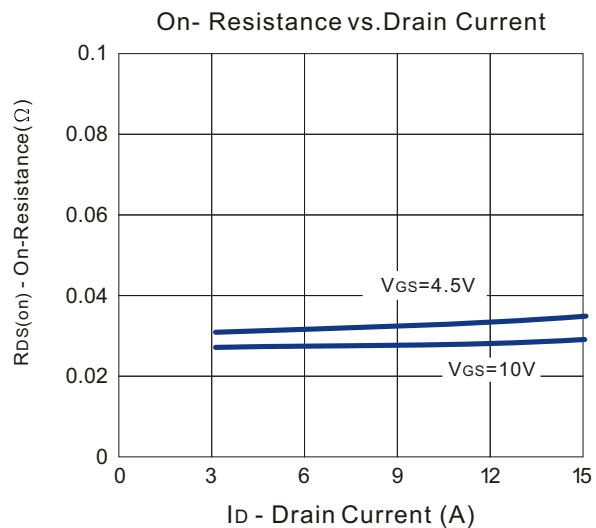
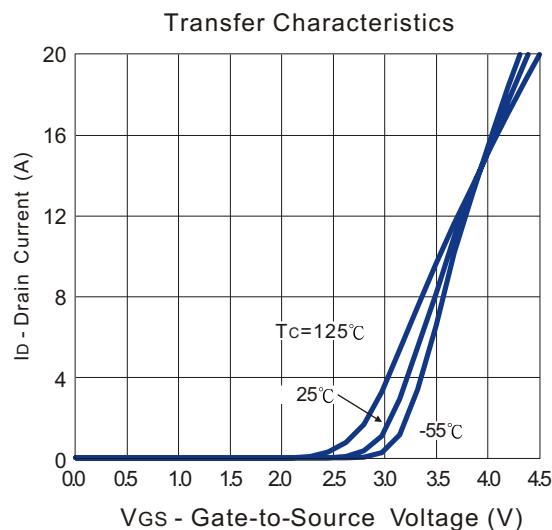
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 10\ \mu\text{A}$	30			V	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	1.21	3.0		
I_{GSS}	Gate-Body Leakage	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA	
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30V, V_{GS} = 0V$			0.5	μA	
		$V_{DS} = 30V, V_{GS} = 0V, T_J = 55^\circ\text{C}$			10		
$I_{D(\text{ON})}$	On-Stae Drain Current ^a	$V_{DS} \geq 4.5V, V_{GS} = 10V$	6			A	
$R_{DS(\text{ON})}$	Drain-Source On-Resistance ^a	$V_{GS} = 10V, I_D = 4.0A$		28	37	$\text{m}\Omega$	
		$V_{GS} = 4.5V, I_D = 3.5A$		36	49		
V_{SD}	Diode Forward Voltage	$I_S = 1.25A, V_{GS} = 0V$		0.8	1.2	V	
DYNAMIC PARAMETERS							
Q_g	Total Gate Charge	$V_{DS} = 15V, V_{GS} = 10V, I_D = 2.5A$		10.6	15	nC	
Q_{gs}	Gate Source Charge			3.2			
Q_{gd}	Gate-Drain Charge			1			
R_g	Gate Resistance	$f = 1.0\text{MHz}$		0.72		Ω	
$t_{d(on)}$	Turn-On Time	$V_{DD} = 15V, R_L = 15\Omega, I_D = 1A, V_{GEN} = 10V, R_G = 6\Omega$		7.4	15	nS	
t_r				13.2	20		
$t_{d(off)}$	Turn-Off Time			21.6	31		
t_f				3.5	9		

Notes

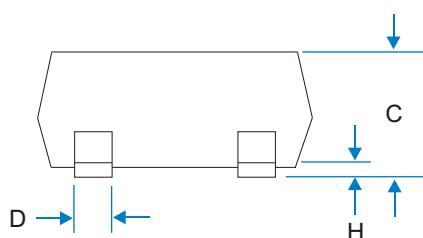
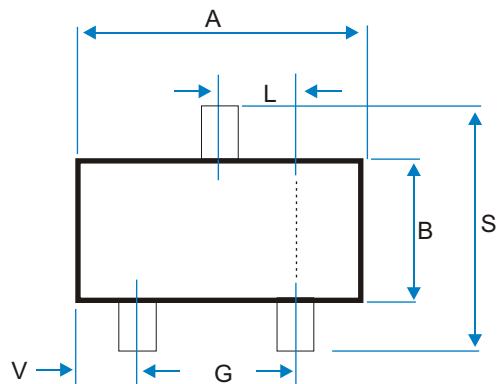
 a. Pulse test: $PW \leq 300\ \mu\text{s}$ duty cycle $\leq 2\%$.

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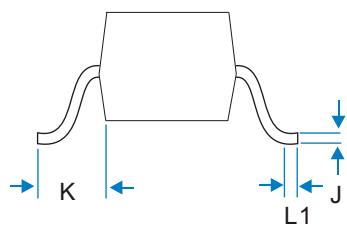
Typical Characteristics ($T_J = 25^\circ\text{C}$ Noted)



SOT-23 Package Outline



DIM	MILLIMETERS	
	MIN	MAX
A	2.80	3.1
B	1.20	1.7
C	0.89	1.3
D	0.37	0.50
G	1.78	2.04
H	0.013	0.15
J	0.085	0.2
K	0.45	0.7
L	0.89	1.02
S	2.10	3
V	0.45	0.60
L1	0.2	0.6



Package Method of Taping

Reel Model	Package	Quality of Reel	Front Blank	Back Blank	Blank Cover
SOT-2X	SOT-23 SOT-25/26/28 SOT26W	3000	20	50	200
SC82	SC82	3000	20	50	200
SOT-89	SOT-89	1000	25	25	75
SOT-223	SOT-223	2500	25	25	75
SOP	SOP8	2500	25	25	75
TSSOP	TSSOP24	2000	25	25	75
TO-252	TO-252	2500	35	35	75
TO-263	TO-263	1000	35	35	75