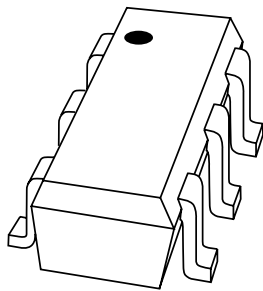


# DATA SHEET



## **PUMD3** NPN/PNP resistor-equipped transistors

Product specification  
Supersedes data of 1998 Nov 26

1999 Apr 13

# NPN/PNP resistor-equipped transistors

# PUMD3

## FEATURES

- Transistors with different polarity and built-in bias resistors R1 and R2 (typ. 10 kΩ each)
- No mutual interference between the transistors
- Simplification of circuit design
- Reduces number of components and board space.

## APPLICATIONS

- Especially suitable for space reduction in interface and driver circuits
- Inverter circuit configurations without use of external resistors.

## DESCRIPTION

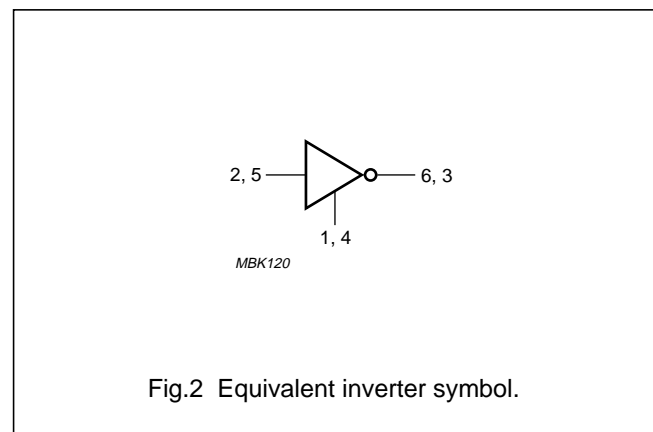
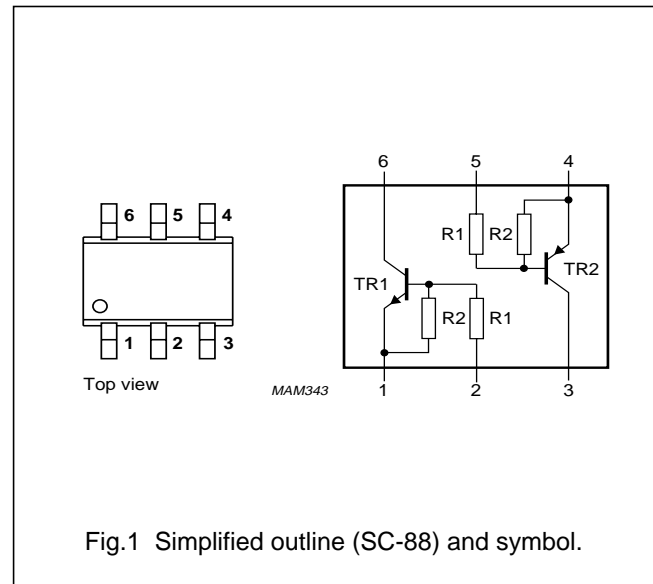
NPN/PNP resistor-equipped transistors in an SC-88 plastic package.

## MARKING

TYPE NUMBER	MARKING CODE
PUMD3	Dt3

## PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



## NPN/PNP resistor-equipped transistors

## PUMD3

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>					
V <sub>CB0</sub>	collector-base voltage	open emitter	–	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	–	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	–	10	V
V <sub>I</sub>	input voltage positive negative		–	+40	V
			–	–10	V
I <sub>O</sub>	output current (DC)		–	100	mA
I <sub>CM</sub>	peak collector current		–	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	200	mW
T <sub>stg</sub>	storage temperature		–65	+150	°C
T <sub>j</sub>	junction temperature		–	150	°C
T <sub>amb</sub>	operating ambient temperature		–65	+150	°C
<b>Per device</b>					
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C; note 1	–	300	mW

**Note**

1. Device mounted on an FR4 printed-circuit board.

## NPN/PNP resistor-equipped transistors

## PUMD3

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	416	K/W

## Note

1. Device mounted on an FR4 printed-circuit board.

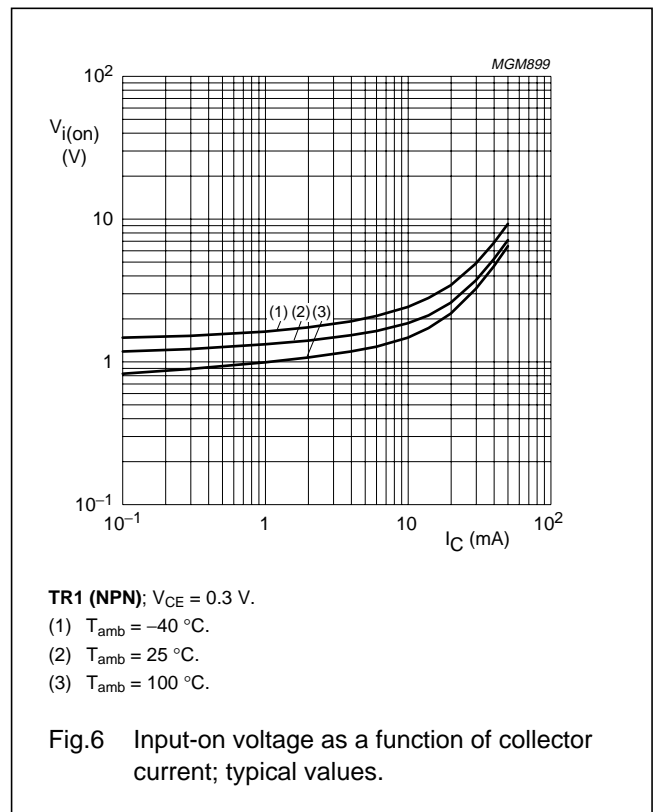
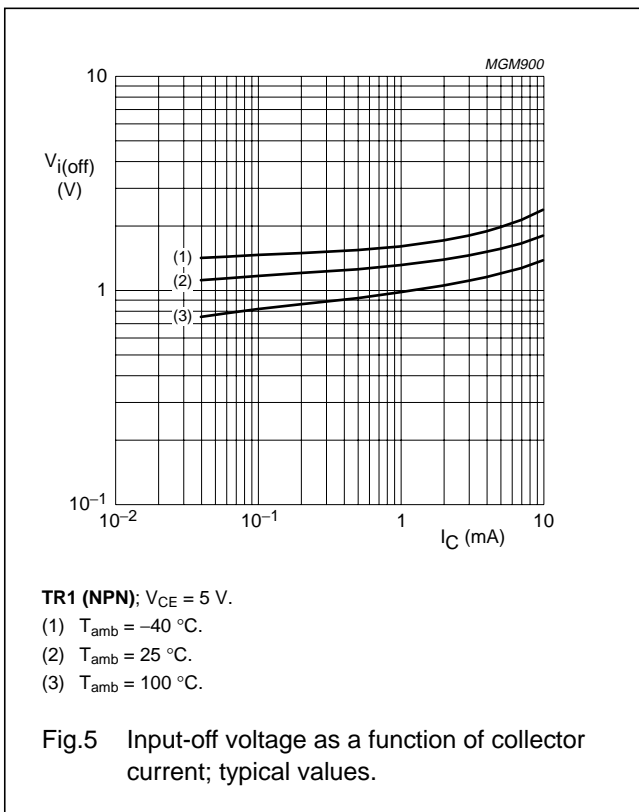
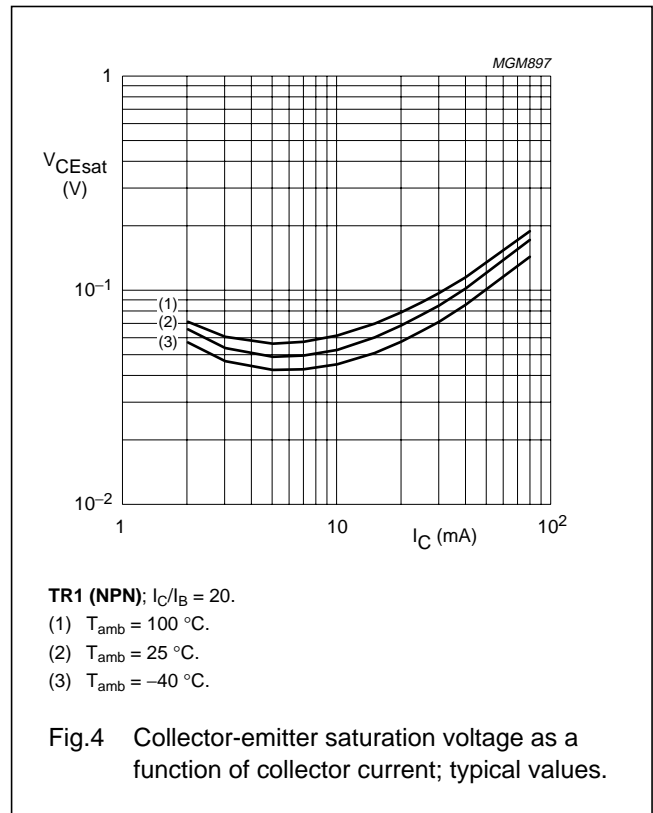
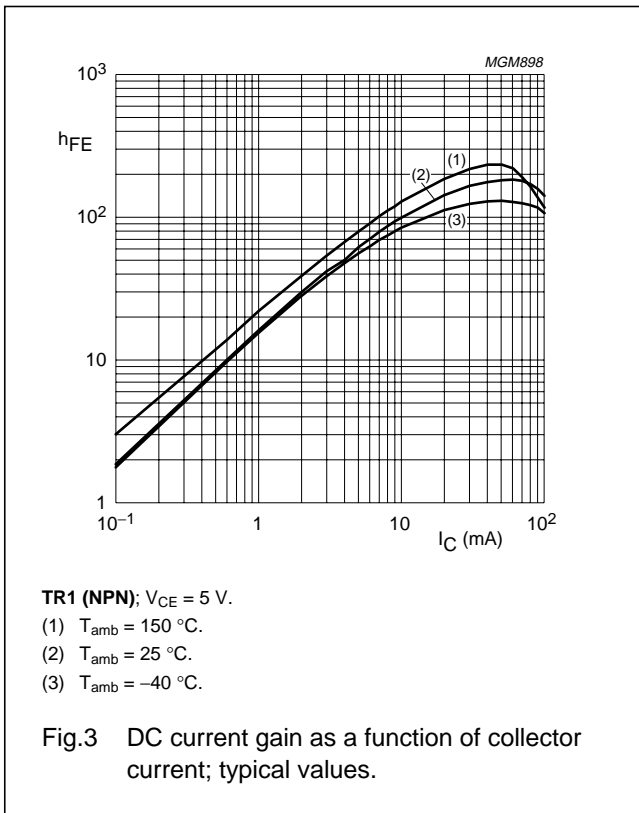
## CHARACTERISTICS

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Per transistor; for the PNP transistor with negative polarity</b>						
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = 50\text{ V}$	–	–	100	nA
$I_{CEO}$	collector cut-off current	$I_B = 0; V_{CE} = 30\text{ V}$	–	–	1	$\mu\text{A}$
		$I_B = 0; V_{CE} = 30\text{ V}; T_j = 150\text{ °C}$	–	–	50	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	400	$\mu\text{A}$
$h_{FE}$	DC current gain	$I_C = 5\text{ mA}; V_{CE} = 5\text{ V}$	30	–	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	–	–	150	mV
$V_{i(off)}$	input-off voltage	$I_C = 100\text{ }\mu\text{A}; V_{CE} = 5\text{ V}$	–	1.1	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = 10\text{ mA}; V_{CE} = 0.3\text{ V}$				
	TR1 (NPN)		2.5	1.8	–	V
	TR2 (PNP)		2.5	1.8	–	V
R1	input resistor		7	10	13	k $\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
$C_c$	collector capacitance	$I_E = I_e = 0; V_{CB} = 10\text{ V};$ $f = 1\text{ MHz}$				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

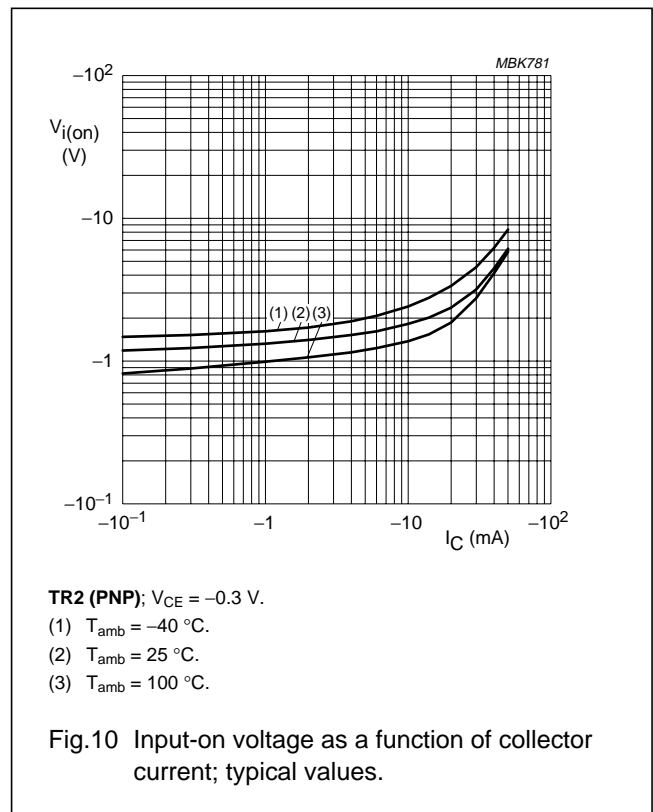
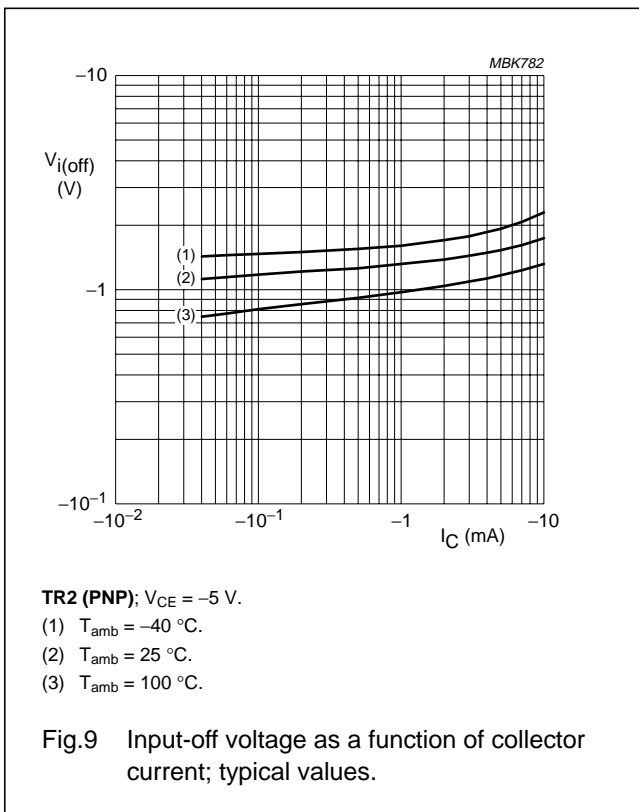
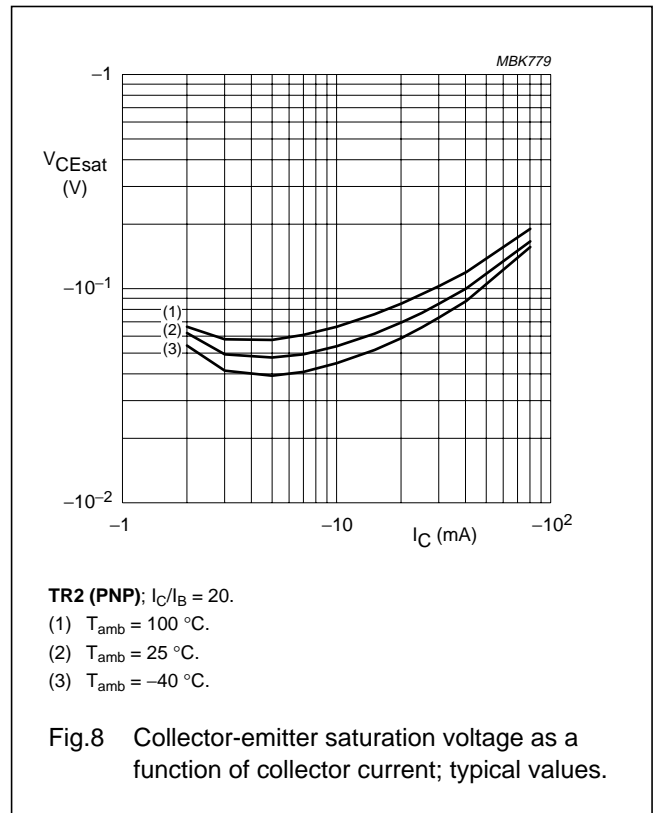
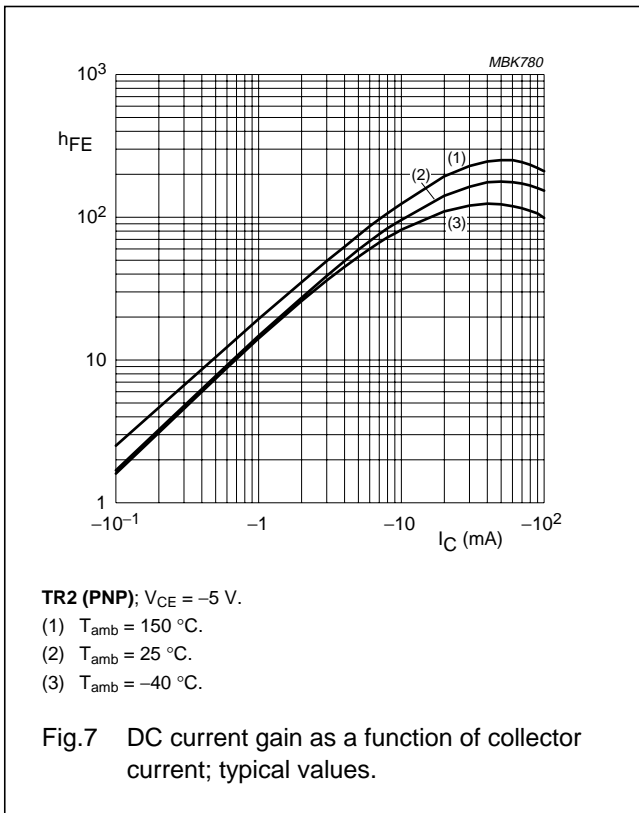
NPN/PNP resistor-equipped transistors

PUMD3



NPN/PNP resistor-equipped transistors

PUMD3



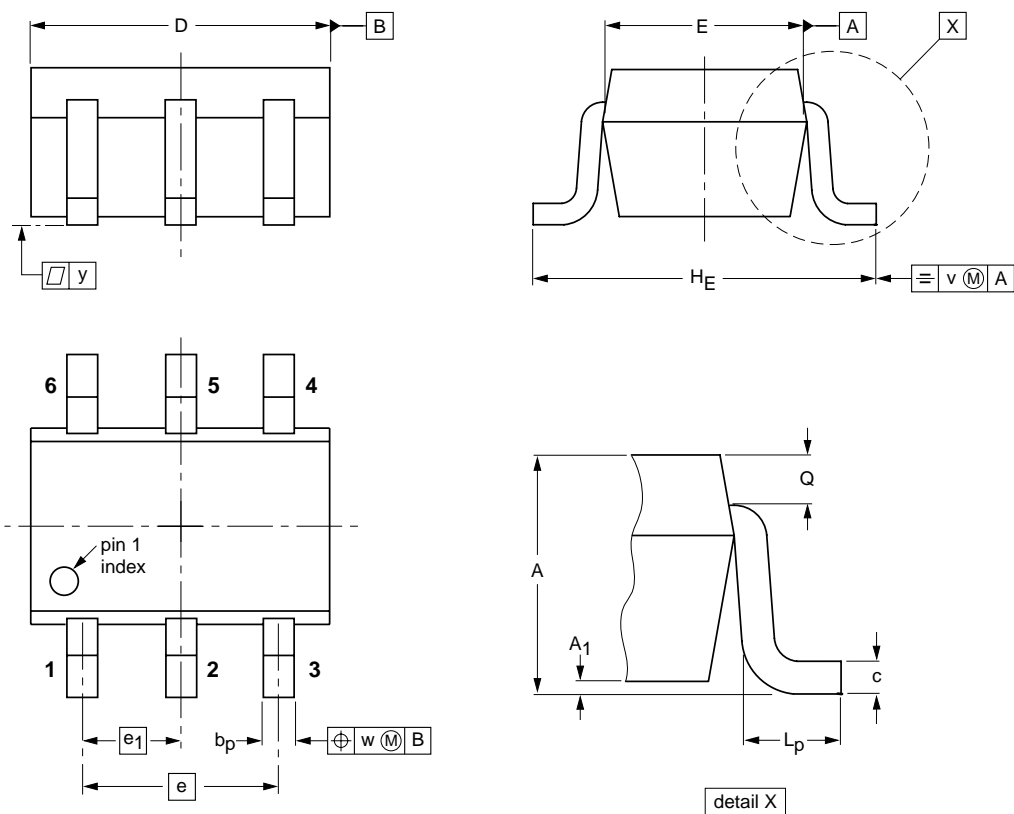
NPN/PNP resistor-equipped transistors

PUMD3

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub> max	b <sub>p</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

## NPN/PNP resistor-equipped transistors

## PUMD3

**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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**NPN/PNP resistor-equipped transistors**

**PUMD3**

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**NOTES**

**NPN/PNP resistor-equipped transistors**

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**NOTES**

**NPN/PNP resistor-equipped transistors**

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
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**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

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**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
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**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Sydhavnsgade 23, 1780 COPENHAGEN V,  
Tel. +45 33 29 3333, Fax. +45 33 29 3905

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615 800, Fax. +358 9 6158 0920

**France:** 51 Rue Carnot, BP317, 92156 SURESNES Cedex,  
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**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
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**India:** Philips INDIA Ltd, Band Box Building, 2nd floor,  
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**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
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**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,  
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,  
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**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
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**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
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**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
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**Norway:** Box 1, Manglerud 0612, OSLO,  
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**Pakistan:** see Singapore

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**South America:** Al. Vicente Pinzon, 173, 6th floor,  
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**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
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**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
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**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
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**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

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