

# Digital transistors (built-in resistor)

## DTD123TK / DTD123TS

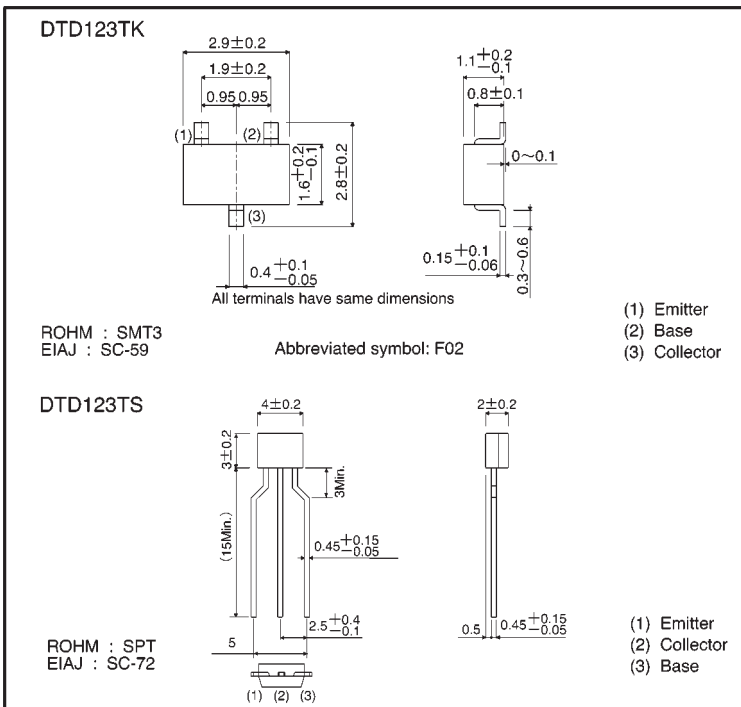
●Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making device design easy.

●Structure

NPN digital transistor  
(Built-in resistor type)

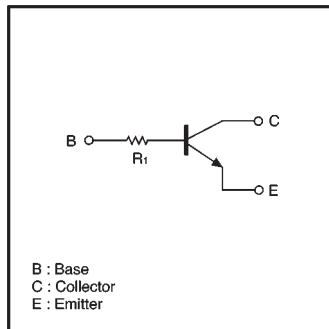
●External dimensions (Units: mm)



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits(DTD123T□)		Unit
		K	S	
Collector-base voltage	V <sub>CBO</sub>	50		V
Collector-emitter voltage	V <sub>CEO</sub>	40		V
Emitter-base voltage	V <sub>EBO</sub>	5		V
Collector current	I <sub>C</sub>	500		mA
Collector power dissipation	P <sub>C</sub>	200	300	mW
Junction temperature	T <sub>j</sub>	150		°C
Storage temperature	T <sub>stg</sub>	-55~+150		°C

●Equivalent circuit



●Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Collector-base breakdown voltage	$BV_{CBO}$	50	—	—	V	$I_C=50\mu A$
Collector-emitter breakdown voltage	$BV_{CEO}$	40	—	—	V	$I_C=1mA$
Emitter-base breakdown voltage	$BV_{EBO}$	5	—	—	V	$I_E=50\mu A$
Collector cutoff current	$I_{CBO}$	—	—	0.5	$\mu A$	$V_{CB}=50V$
Emitter cutoff current	$I_{EBO}$	—	—	0.5	$\mu A$	$V_{EB}=4V$
Collector-emitter saturation voltage	$V_{CE(sat)}$	—	—	0.3	V	$I_C/I_B=50m/2.5mA$
DC current transfer ratio	$h_{FE}$	100	250	600	—	$V_{CE}=5V, I_C=50mA$
Input resistance	$R_i$	1.54	2.2	2.86	k $\Omega$	—
Transition frequency	$f_T$	—	200	—	MHz	$V_{CE}=10V, I_E=-50mA, f=100MHz$ *

\* Transition frequency of the device

●Packaging specifications

Part No.	Package	SMT3	SPT
	Packaging type	Taping	Taping
	Code	T146	TP
	Basic ordering unit (pieces)	3000	5000
DTD123TK		○	—
DTD123TS		—	○

●Electrical characteristic curves

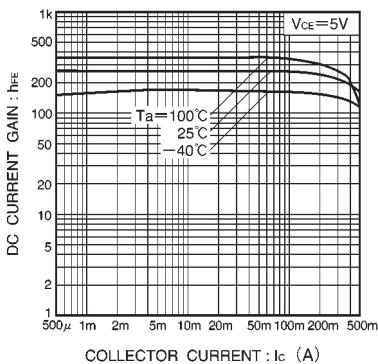


Fig.1 DC current gain vs. collector current

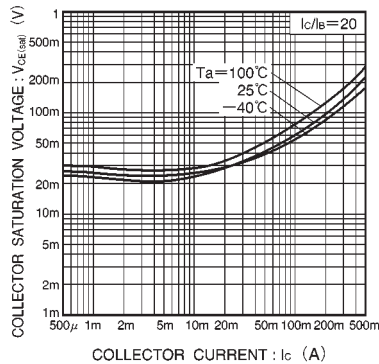


Fig.2 Collector-emitter saturation voltage vs. collector current