# MC74VHC1GT125

# Noninverting Buffer / CMOS Logic Level Shifter
## with LSTTL−Compatible Inputs

The MC74VHC1GT125 is a single gate noninverting buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC1GT125 requires the 3−state control input ($\overline{OE}$) to be set High to place the output into the high impedance state.

The device input is compatible with TTL−type input thresholds and the output has a full 5.0 V CMOS level output swing. The input protection circuitry on this device allows overvoltage tolerance on the input, allowing the device to be used as a logic−level translator from 3.0 V CMOS logic to 5.0 V CMOS Logic or from 1.8 V CMOS logic to 3.0 V CMOS Logic while operating at the high−voltage power supply.

The MC74VHC1GT125 input structure provides protection when voltages up to 7.0 V are applied, regardless of the supply voltage. This allows the MC74VHC1GT125 to be used to interface 5.0 V circuits to 3.0 V circuits. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage − input/output voltage mismatch, battery backup, hot insertion, etc.

### Features

- High Speed: $t_{PD}$ = 3.5 ns (Typ) at $V_{CC}$ = 5 V
- Low Power Dissipation: $I_{CC}$ = 1 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2.0 V
- CMOS−Compatible Outputs: $V_{OH}$ > 0.8 $V_{CC}$; $V_{OL}$ < 0.1 $V_{CC}$ @Load
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 62; Equivalent Gates = 16
- Pb−Free Packages are Available

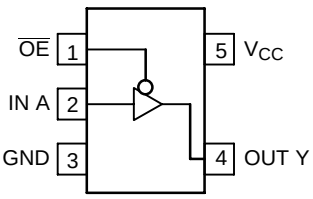



**Figure 1. Pinout** (Top View)

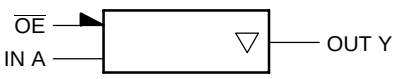


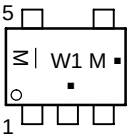

**Figure 2. Logic Symbol**

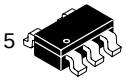
**ON Semiconductor®**

**http://onsemi.com**

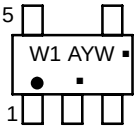
**MARKING DIAGRAMS**


**SC−88A/SOT−353/SC−70**
**DF SUFFIX**
**CASE 419A**




**TSOP−5/SOT−23/SC−59**
**DT SUFFIX**
**CASE 483**




W1 = Device Code
M = Date Code*
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

| PIN ASSIGNMENT | |
|---|---|
| 1 | $\overline{OE}$ |
| 2 | IN A |
| 3 | GND |
| 4 | OUT Y |
| 5 | $V_{CC}$ |

**FUNCTION TABLE**

| A Input | $\overline{OE}$ Input | Y Output |
|---|---|---|
| L | L | L |
| H | L | H |
| X | H | Z |

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

**MAXIMUM RATINGS**

| Symbol | Characteristics | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | DC Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | $V_{CC}$ = 0<br>High or Low State | −0.5 to 7.0<br>−0.5 to $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | $V_{OUT}$ < GND; $V_{OUT}$ > $V_{CC}$ | +20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | | +25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND | | +50 | mA |
| $P_D$ | Power Dissipation in Still Air | SC−88A, TSOP−5 | 200 | mW |
| $\theta_{JA}$ | Thermal Resistance | SC−88A, TSOP−5 | 333 | °C/W |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 s | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | +150 | °C |
| $T_{stg}$ | Storage Temperature | | −65 to +150 | °C |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | > 2000<br>> 200<br>N/A | V |
| $I_{Latchup}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 4) | ±500 | mA |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 3.0 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | | 0.0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | | 0.0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −55 | +125 | °C |
| $t_r$ , $t_f$ | Input Rise and Fall Time | $V_{CC}$ = 5.0 V ± 0.5 V | 0 | 20 | ns/V |

**Device Junction Temperature versus Time to 0.1% Bond Failures**

| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

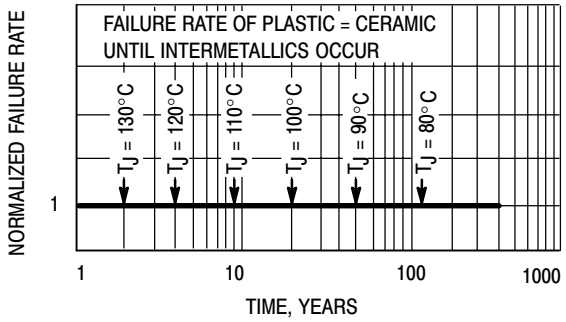



**Figure 3. Failure Rate vs. Time Junction Temperature**

## DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | $T_A$ = 25°C | | | $T_A \le$ 85°C | | −55 ≤ $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| $V_{IH}$ | Minimum High−Level Input Voltage | | 3.0<br>4.5<br>5.5 | 1.4<br>2.0<br>2.0 | | | 1.4<br>2.0<br>2.0 | | 1.4<br>2.0<br>2.0 | | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | | 3.0<br>4.5<br>5.5 | | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | | 0.53<br>0.8<br>0.8 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 50 μA | 3.0<br>4.5 | 2.9<br>4.4 | 3.0<br>4.5 | | 2.9<br>4.4 | | 2.9<br>4.4 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OH}$ = − 4 mA<br>$I_{OH}$ = − 8 mA | 3.0<br>4.5 | 2.58<br>3.94 | | | 2.48<br>3.80 | | 2.34<br>3.66 | | |
| $V_{OL}$ | Maximum Low−Level Output Voltage $V_{IN} = V_{IH}$ or $V_{IL}$ | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 50 μA | 3.0<br>4.5 | | 0.0<br>0.0 | 0.1<br>0.1 | | 0.1<br>0.1 | | 0.1<br>0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$I_{OL}$ = 4 mA<br>$I_{OL}$ = 8 mA | 3.0<br>4.5 | | | 0.36<br>0.36 | | 0.44<br>0.44 | | 0.52<br>0.52 | |
| $I_{IN}$ | Maximum Input Leakage Current | $V_{IN}$ = 5.5 V or GND | 0 to 5.5 | | | ± 0.10 | | ± 1.0 | | ± 1.0 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.0 | | 20 | | 40 | μA |
| $I_{CCT}$ | Quiescent Supply Current | Input: $V_{IN}$ = 3.4 V<br>Other Input: $V_{CC}$ or GND | 5.5 | | | 1.35 | | 1.50 | | 1.65 | mA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT}$ = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |
| $I_{OZ}$ | Maximum 3−State Leakage Current | $V_{IN} = V_{IH}$ or $V_{IL}$<br>$V_{OUT} = V_{CC}$ or GND | 5.5 | | | ± 0.25 | | ± 2.5 | | ± 2.5 | μA |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT}$ = 5.5 V | 0.0 | | | 0.5 | | 5.0 | | 10 | μA |

## AC ELECTRICAL CHARACTERISTICS Input $t_r = t_f$ = 3.0 ns

| Symbol | Parameter | Test Conditions | $T_A$ = 25°C | | | $T_A \le$ 85°C | | −55 ≤ $T_A \le$ 125°C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A to Y (Figures 3 and 5.) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15pF<br>$C_L$ = 50pF | | 5.6<br>8.1 | 8.0<br>11.5 | 1.0<br>1.0 | 9.5<br>13.0 | | 12.0<br>16.0 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15pF<br>$C_L$ = 50pF | | 3.8<br>5.3 | 5.5<br>7.5 | 1.0<br>1.0 | 6.5<br>8.5 | | 8.5<br>10.5 | |
| $t_{PZL}$, $t_{PZH}$ | Maximum Output Enable TIme, $\overline{OE}$ to Y (Figures 4 and 5) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50pF | | 5.4<br>7.9 | 8.0<br>11.5 | 1.0<br>1.0 | 9.5<br>13.0 | | 11.5<br>15.0 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50pF | | 3.6<br>5.1 | 5.1<br>7.1 | 1.0<br>1.0 | 6.0<br>8.0 | | 7.5<br>9.5 | |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Output Disable Time, $\overline{OE}$ to Y (Figures 4 and 5) | $V_{CC}$ = 3.3 ± 0.3 V $C_L$ = 15pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50pF | | 6.5<br>8.0 | 9.7<br>13.2 | 1.0<br>1.0 | 11.5<br>15.0 | | 14.5<br>18.0 | ns |
| | | $V_{CC}$ = 5.0 ± 0.5 V $C_L$ = 15pF<br>$R_L = R_I$ = 500 Ω $C_L$ = 50pF | | 4.8<br>7.0 | 6.8<br>8.8 | 1.0<br>1.0 | 8.0<br>10.0 | | 10.0<br>12.0 | |
| $C_{in}$ | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |
| $C_{out}$ | Maximum Three−State Output Capacitance (Output in High Impedance State) | | | 6 | | | | | | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | 14 | pF |

5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/4$ (per buffer). $C_{PD}$ is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## SWITCHING WAVEFORMS

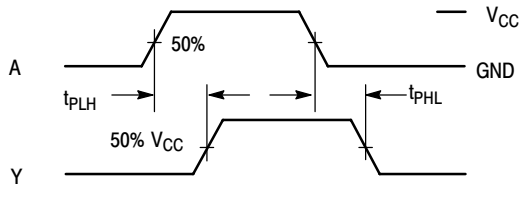



**Figure 4. Switching Waveforms**

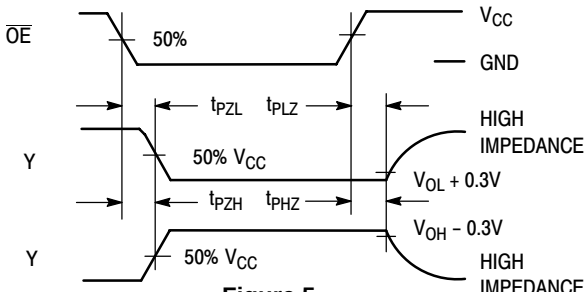
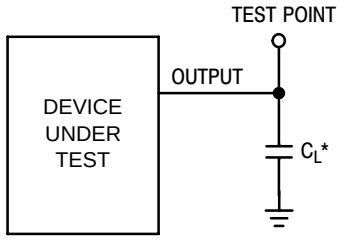
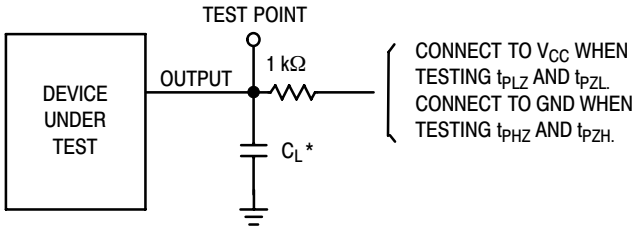



**Figure 5.**




*Includes all probe and jig capacitance

**Figure 6. Test Circuit**




*Includes all probe and jig capacitance

**Figure 7. Test Circuit**

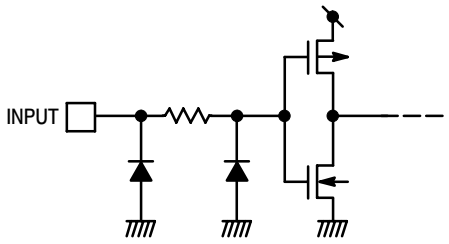



**Figure 8. Input Equivalent Circuit**

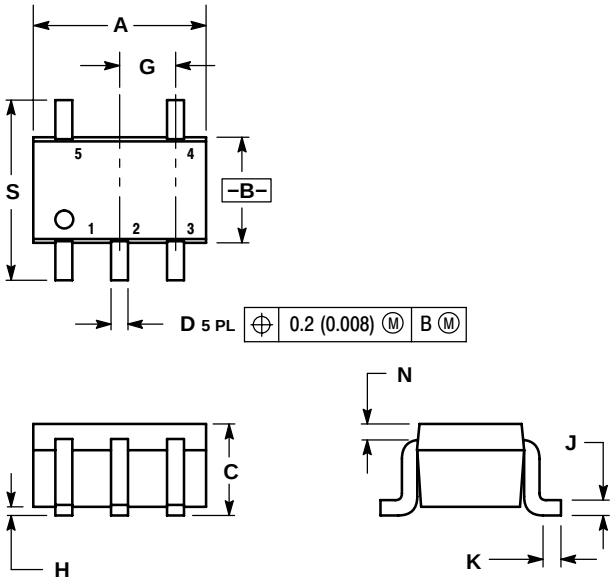
### DEVICE ORDERING INFORMATION

| Device Order Number | Package Type | Tape and Reel Size† |
|---|---|---|
| MC74VHC1GT125DF1 | SC−88A / SOT−353 / SC−70 | 178 mm (7”) 3000 Units / Tape & Reel |
| M74VHC1GT125DF1G | SC−88A / SOT−353 / SC−70 (Pb−Free) | |
| MC74VHC1GT125DF2 | SC−88A / SOT−353 / SC−70 | |
| M74VHC1GT125DF2G | SC−88A / SOT−353 / SC−70 (Pb−Free) | |
| MC74VHC1GT125DT1 | TSOP−5 / SOT−23 / SC−59 | |
| M74VHC1GT125DT1G | TSOP−5 / SOT−23 / SC−59 (Pb−Free) | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## PACKAGE DIMENSIONS

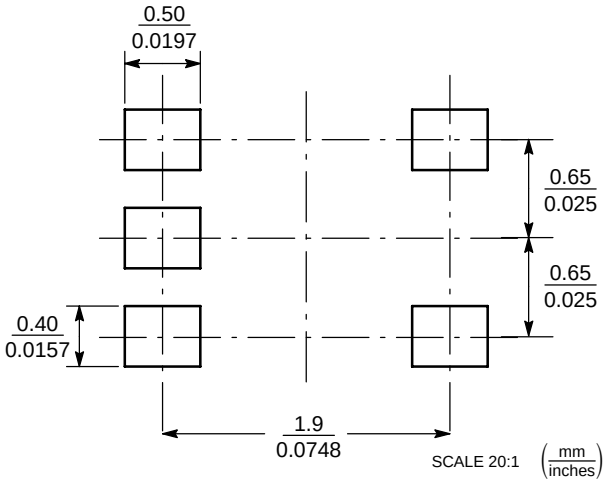
**SC70−5/SC−88A/SOT−353**
**DF SUFFIX**
CASE 419A−02
ISSUE H




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A−01 OBSOLETE. NEW STANDARD 419A−02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |

### SOLDERING FOOTPRINT*

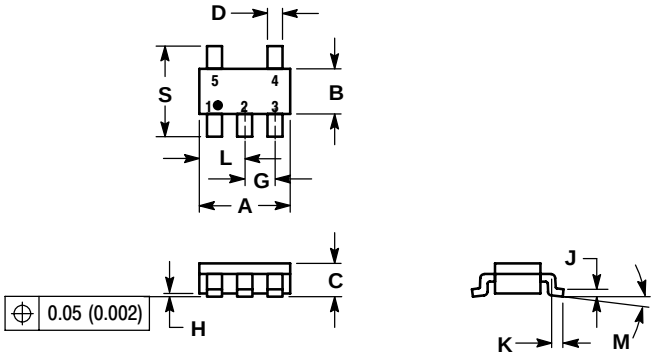



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC74VHC1GT125

## PACKAGE DIMENSIONS

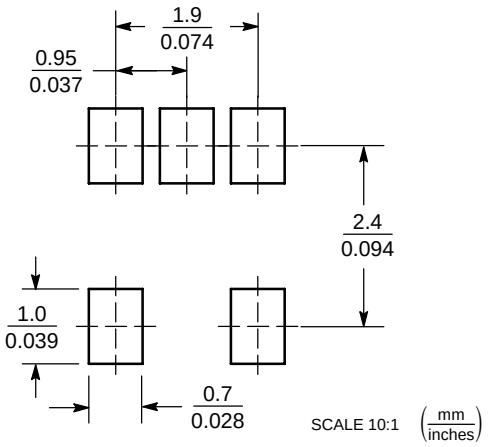
**SOT23−5/TSOP−5/SC59−5**
**DT SUFFIX**
CASE 483−02
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. A AND B DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.1142 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 0.90 | 1.10 | 0.0354 | 0.0433 |
| D | 0.25 | 0.50 | 0.0098 | 0.0197 |
| G | 0.85 | 1.05 | 0.0335 | 0.0413 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.10 | 0.26 | 0.0040 | 0.0102 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.55 | 0.0493 | 0.0610 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

## SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**PUBLICATION ORDERING INFORMATION**

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
**Phone**: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
**Fax**: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada

**Japan**: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
**Phone**: 81−3−5773−3850

**ON Semiconductor Website**: http://onsemi.com

**Order Literature**: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

**MC74VHC1GT125/D**