MBT35200MT1

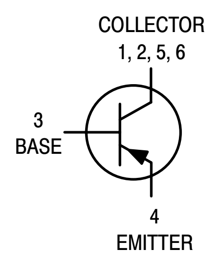
High Current Surface Mount PNP Silicon Switching Transistor for Load Management in Portable Applications

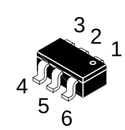
A Device of the µ*X*™ Family

ON Semiconductor

http://onsemi.com

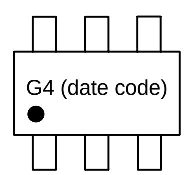
35 VOLTS
2.0 AMPS
PNP TRANSISTOR





CASE 318G
TSOP
STYLE 6

DEVICE MARKING



MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	–35	Vdc
Collector-Base Voltage	V_{CBO}	–55	Vdc
Emitter-Base Voltage	V_{EBO}	–5.0	Vdc
Collector Current — Continuous	I_C	–2.0	Adc
Collector Current — Peak	I_{CM}	–5.0	A
Electrostatic Discharge	ESD	HBM Class 3 MM Class C	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1.)	625 5.0	mW mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 1.)	200	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2.)	1.0 8.0	W mW/°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$ (Note 2.)	120	°C/W
Thermal Resistance, Junction to Lead #1	$R_{\theta JL}$	80	°C/W
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{Dsingle}$ (Notes 2. & 3.)	1.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C

1. FR–4 @ Minimum Pad
2. FR–4 @ 1.0 X 1.0 inch Pad
3. ref: Figure 9

ORDERING INFORMATION

Device	Package	Shipping
MBT35200MT1	Case 318G	3000/Tape & Reel

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = –10 mAdc, I_B = 0)	$V_{(BR)CEO}$	–35	–45	—	Vdc
Collector–Base Breakdown Voltage (I_C = –0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	–55	–65	—	Vdc
Emitter–Base Breakdown Voltage (I_E = –0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	–5.0	–7.0	—	Vdc
Collector Cutoff Current (V_{CB} = –35 Vdc, I_E = 0)	I_{CBO}	—	–0.03	–0.1	μAdc
Collector–Emitter Cutoff Current (V_{CES} = –35 Vdc)	I_{CES}	—	–0.03	–0.1	μAdc
Emitter Cutoff Current (V_{EB} = –4.0 Vdc)	I_{EBO}	—	–0.01	–0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (1)	h_{FE}				
(I_C = –1.0 A, V_{CE} = –1.5 V)		100	200	—	
(I_C = –1.5 A, V_{CE} = –1.5 V)		100	200	400	
(I_C = –2.0 A, V_{CE} = –3.0 V)		100	200	—	
Collector–Emitter Saturation Voltage (Note 4.)	$V_{CE(sat)}$				V
(I_C = –0.8 A, I_B = –0.008 A)		—	–0.125	–0.15	
(I_C = –1.2 A, I_B = –0.012 A)		—	–0.175	–0.20	
(I_C = –2.0 A, I_B = –0.02 A)		—	–0.260	–0.31	
Base–Emitter Saturation Voltage (Note 4.) (I_C = –1.2 A, I_B = –0.012 A)	$V_{BE(sat)}$	—	–0.68	–0.85	V
Base–Emitter Turn–on Voltage (Note 4.) (I_C = –2.0 A, V_{CE} = –3.0 V)	$V_{BE(on)}$	—	–0.81	–0.875	V
Cutoff Frequency (I_C = –100 mA, V_{CE} = –5.0 V, f = 100 MHz)	f_T	100	—	—	MHz
Input Capacitance (V_{EB} = –0.5 V, f = 1.0 MHz)	Cibo	—	600	650	pF
Output Capacitance (V_{CB} = –3.0 V, f = 1.0 MHz)	Cobo	—	85	100	pF
Turn–on Time (V_{CC} = –10 V, I_{B1} = –100 mA, I_C = –1 A, R_L = 3 Ω)	t_{on}	—	35	—	nS
Turn–off Time (V_{CC} = –10 V, I_{B1} = I_{B2} = –100 mA, I_C = 1 A, R_L = 3 Ω)	t_{off}	—	225	—	nS

4. Pulsed Condition: Pulse Width = 300 μsec, Duty Cycle ≤ 2%

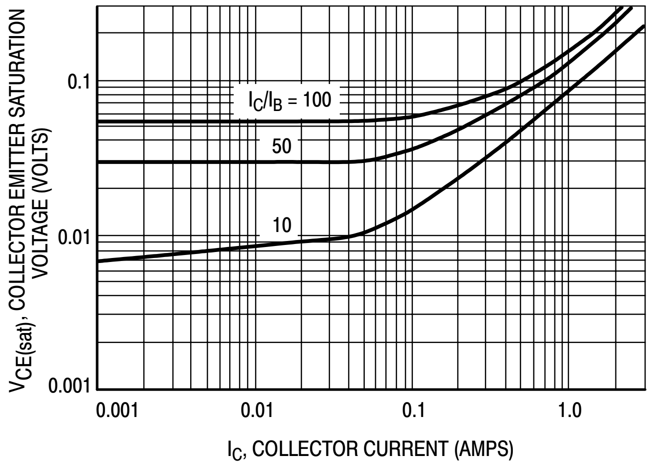


Figure 1. Collector Emitter Saturation Voltage versus Collector Current

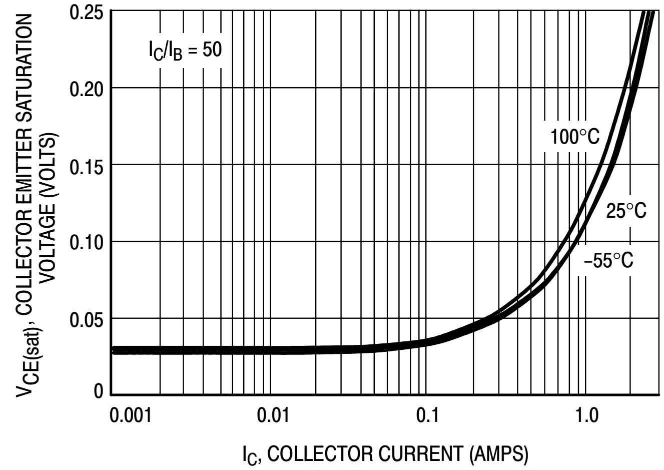


Figure 2. Collector Emitter Saturation Voltage versus Collector Current

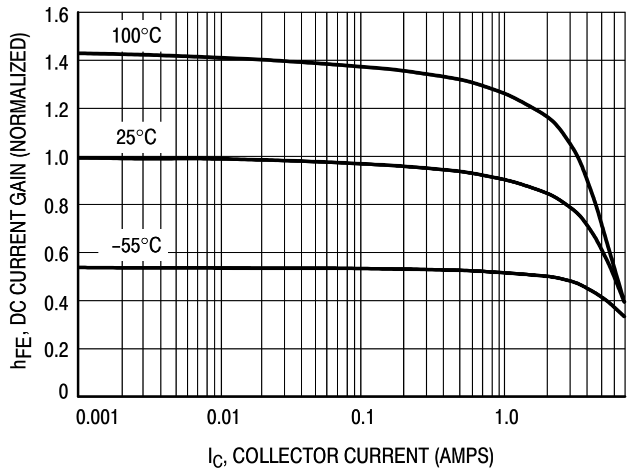


Figure 3. DC Current Gain versus Collector Current

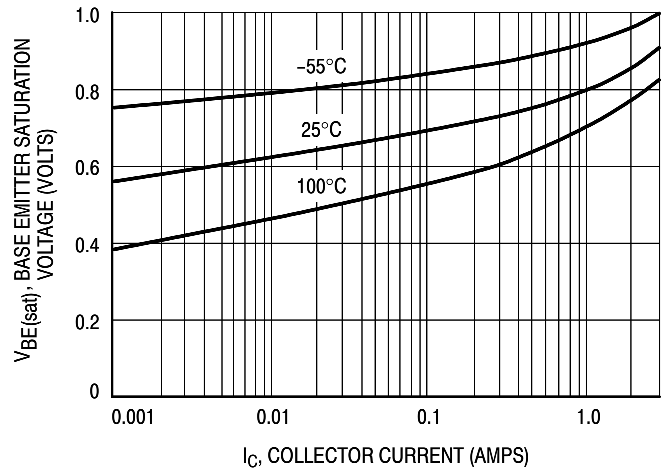


Figure 4. Base Emitter Saturation Voltage versus Collector Current

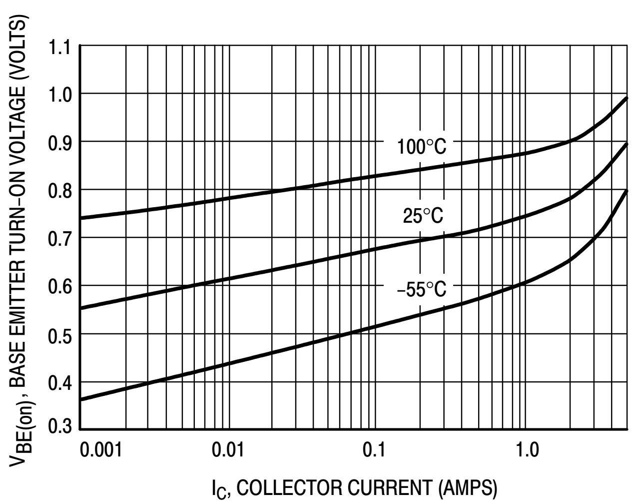


Figure 5. Base Emitter Turn−On Voltage versus Collector Current

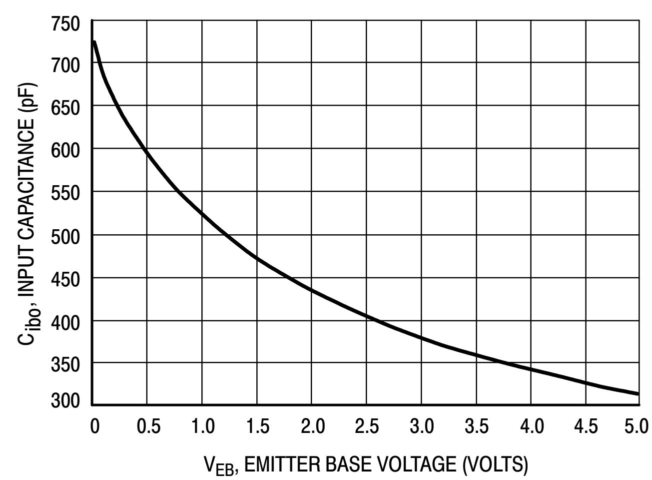


Figure 6. Input Capacitance

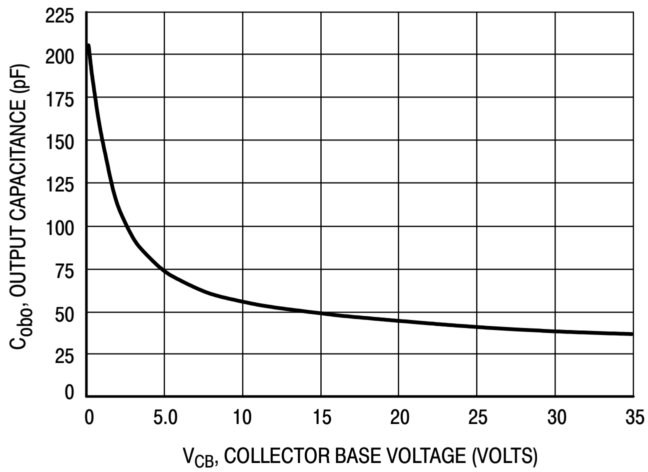


Figure 7. Output Capacitance

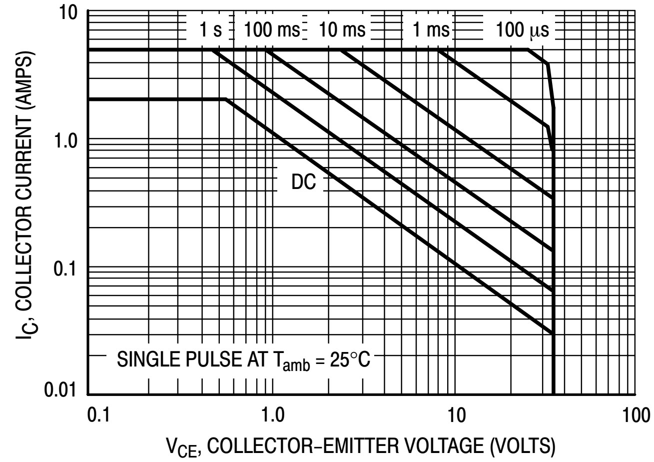


Figure 8. Safe Operating Area

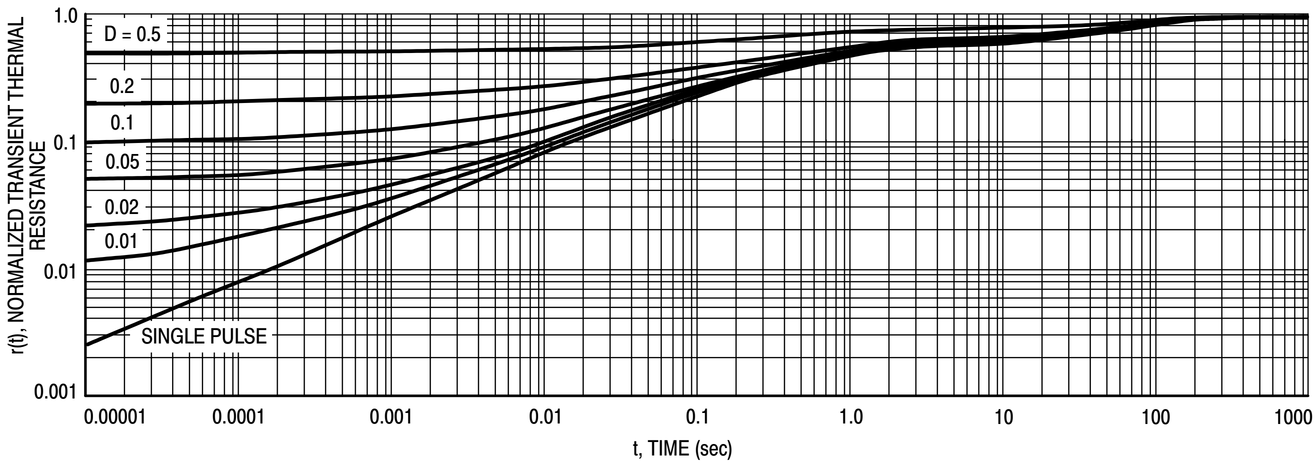
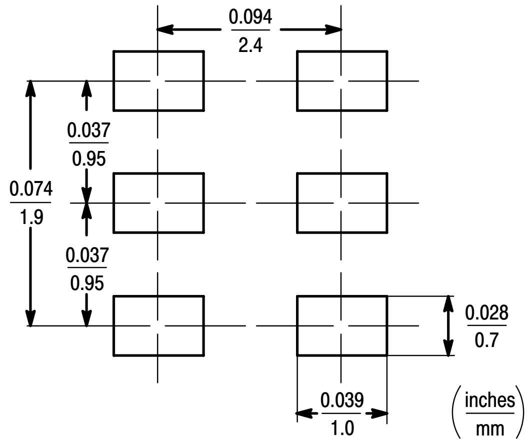


Figure 9. Normalized Thermal Response

INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



TSOP–6

TSOP–6 POWER DISSIPATION

The power dissipation of the TSOP–6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the TSOP–6 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 625 milliwatts.

$$P_D = \frac{150°C - 25°C}{200°C/W} = 625 \text{ milliwatts}$$

The 200°C/W for the TSOP–6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 625 milliwatts. There are other alternatives to achieving higher power dissipation from the TSOP–6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

SOLDERING PRECAUTIONS

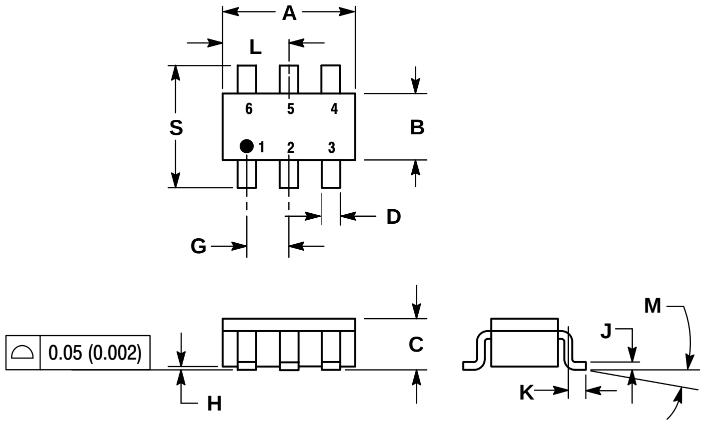
The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS

CASE 318G–02
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.1142	0.1220
B	1.30	1.70	0.0512	0.0669
C	0.90	1.10	0.0354	0.0433
D	0.25	0.50	0.0098	0.0197
G	0.85	1.05	0.0335	0.0413
H	0.013	0.100	0.0005	0.0040
J	0.10	0.26	0.0040	0.0102
K	0.20	0.60	0.0079	0.0236
L	1.25	1.55	0.0493	0.0610
M	0 °	10 °	0 °	10 °
S	2.50	3.00	0.0985	0.1181

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

Notes

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