MMFT3055E

Power MOSFET
1.7 Amp, 60 Volts
N−Channel TMOS E−FET™ SOT−223

This advanced E−FET is a TMOS Medium Power MOSFET designed to withstand high energy in the avalanche and commutation modes. This new energy efficient device also offers a drain−to−source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, dc−dc converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

Features

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.15 Ω max
- The SOT−223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
  Use MMFT3055ET1 to order the 7 inch/1000 unit reel.
  Use MMFT3055ET3 to order the 13 inch/4000 unit reel.

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Gate−to−Source Voltage− Continuous	V_{GS}	± 20	Vdc
Drain Current − Continuous − Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	1.7 6.8	Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C (Note 1)	P_D	0.8 6.3	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 60 Vdc, V_{GS} = 10 Vdc, Peak I_L = 1.7 Apk, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	168	mJ
Thermal Resistance − Junction to Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

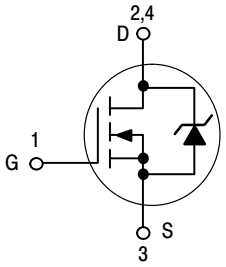
1. Power rating when mounted on FR−4 glass epoxy printed circuit board using recommended footprint.

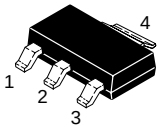
ON Semiconductor®

http://onsemi.com

V_{DSS}	$R_{DS(ON)}$ TYP	I_D MAX
60 V	150 mΩ	1.7 A

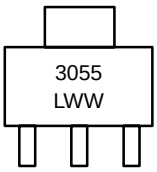
N−Channel





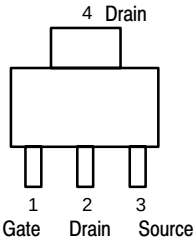
SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



L = Location Code
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
MMFT3055ET1	SOT−223	1000 Tape & Reel
MMFT3055ET3	SOT−223	4000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	60			Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 60 V, V_{GS} = 0 V)		I_{DSS}			10	μAdc
Gate−Body Leakage Current, (V_{GS} = 20 V, V_{DS} = 0 V)		I_{GSS}			100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	2.0		4.5	Vdc
Static Drain−to−Source On−Resistance, (V_{GS} = 10 V, I_D = 0.85 A)		$R_{DS(on)}$			0.15	Ω
Drain−to−Source On−Voltage, (V_{GS} = 10 V, I_D = 1.7 A)		$V_{DS(on)}$			0.34	Vdc
Forward Transconductance, (V_{DS} = 15 V, I_D = 0.85 A)		g_{FS}		2.2		mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}		430		pF
Output Capacitance		C_{oss}		225		
Reverse Transfer Capacitance		C_{rss}		40		
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	(V_{DD} = 25 V, I_D = 0.85 A V_{GS} = 10 V, R_G = 50 Ω, R_{GS} = 25 Ω)	$t_{d(on)}$		15		ns
Rise Time		t_r		22		
Turn−Off Delay Time		$t_{d(off)}$		31		
Fall Time		t_f		49		
Total Gate Charge	(V_{DS} = 48 V, I_D = 1.7 A, V_{GS} = 10 Vdc) See Figures 15 and 16	Q_g		12.5		nC
Gate−Source Charge		Q_{gs}		2.0		
Gate−Drain Charge		Q_{gd}		4.5		
SOURCE DRAIN DIODE CHARACTERISTICS(1)						
Forward On−Voltage	I_S = 1.7 A, V_{GS} = 0 V	V_{SD}		0.8		Vdc
Forward Turn−On Time	I_S = 1.7 A, V_{GS} = 0 V, dI_S/dt = 400 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}		50		ns

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

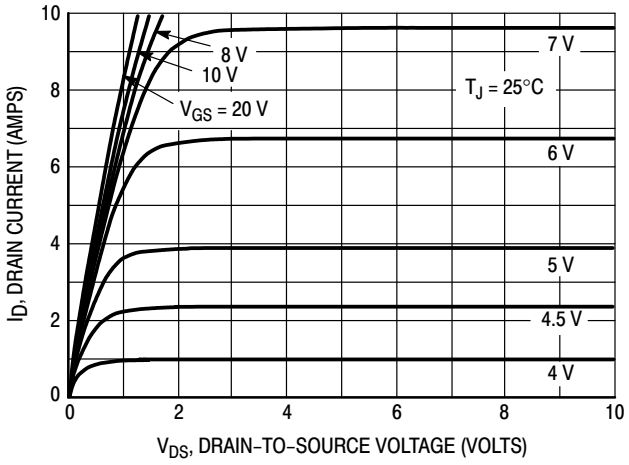


Figure 1. On Region Characteristics

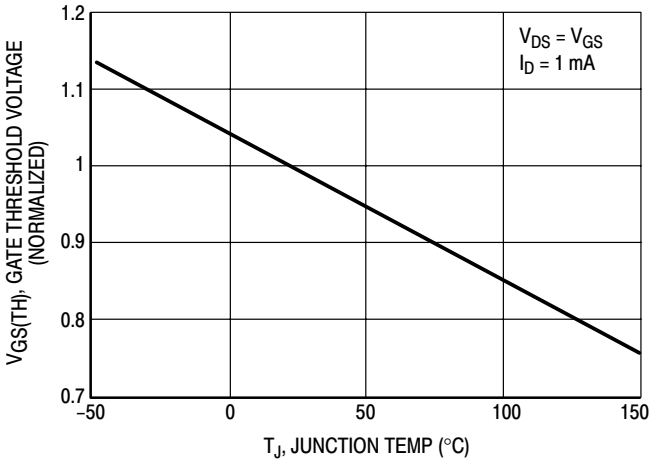


Figure 2. Gate−Threshold Voltage Variation With Temperature

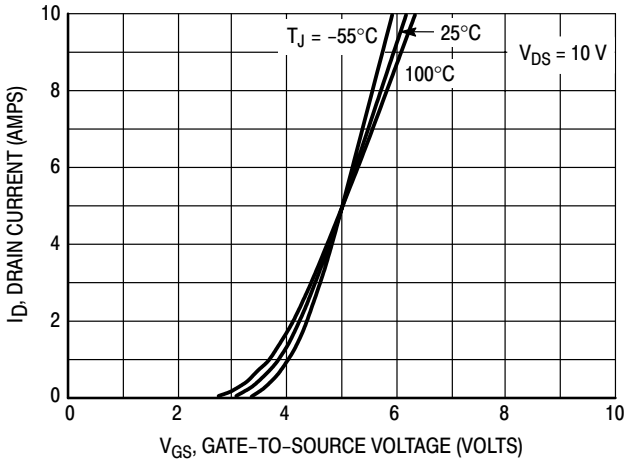


Figure 3. Transfer Characteristics

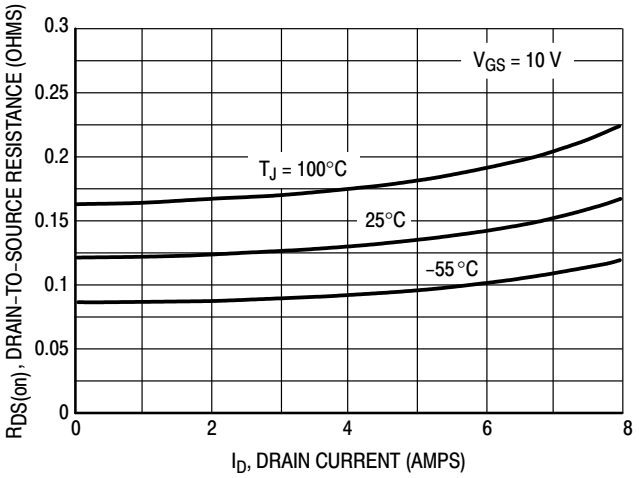


Figure 4. On−Resistance versus Drain Current

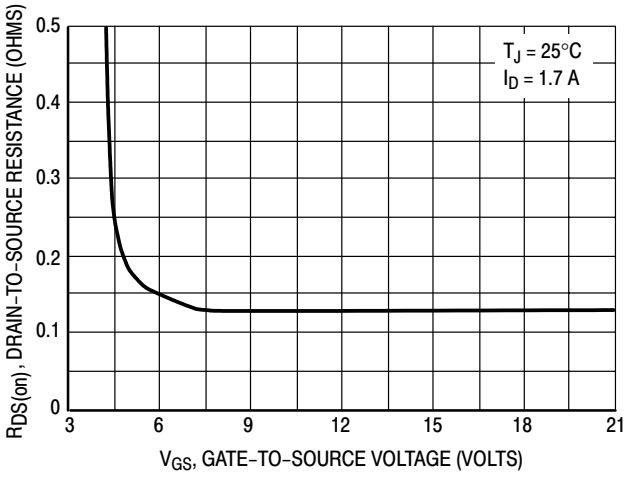


Figure 5. On−Resistance versus Gate−to−Source Voltage

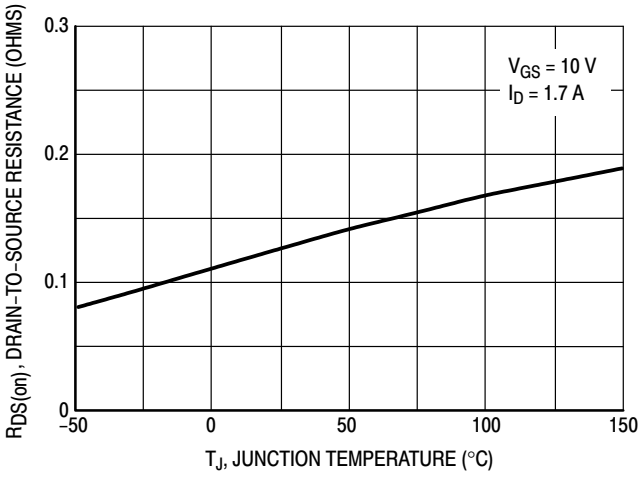


Figure 6. On−Resistance versus Junction Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain−to−source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on an ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. Application Note, AN569, “Transient Thermal Resistance−General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA is applicable for both turn−on and turn−off of the devices for switching times less than one microsecond.

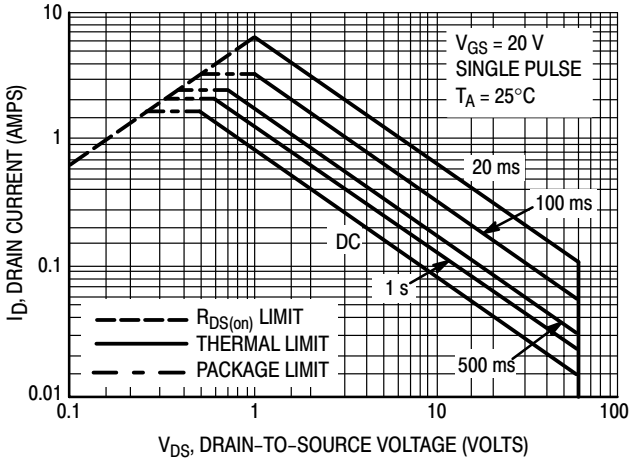


Figure 7. Maximum Rated Forward Biased Safe Operating Area

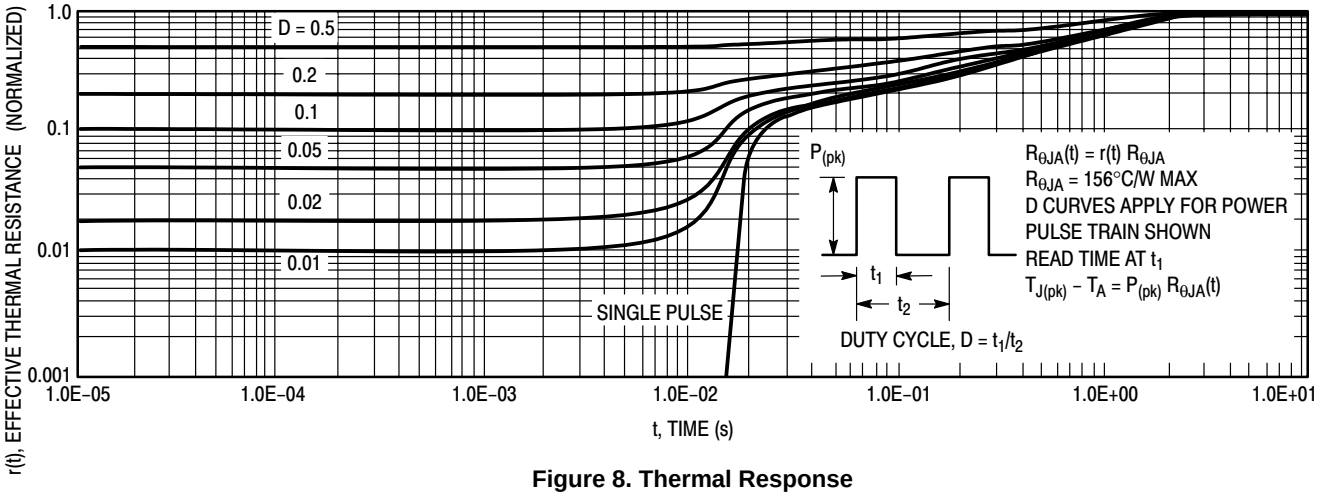


Figure 8. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source−drain current versus re−applied drain voltage when the source−drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half−bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain−to−source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source−drain diode current just prior to the onset of commutation.

V_R is specified at 80% rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in ON Semiconductor’s test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

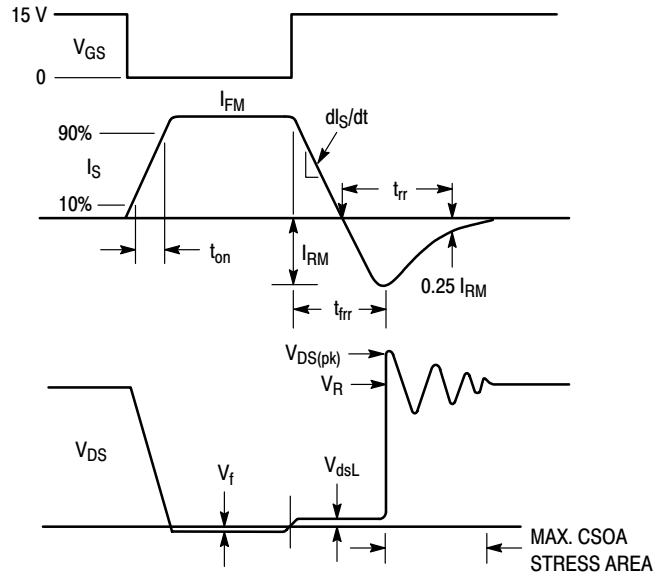


Figure 9. Commutating Waveforms

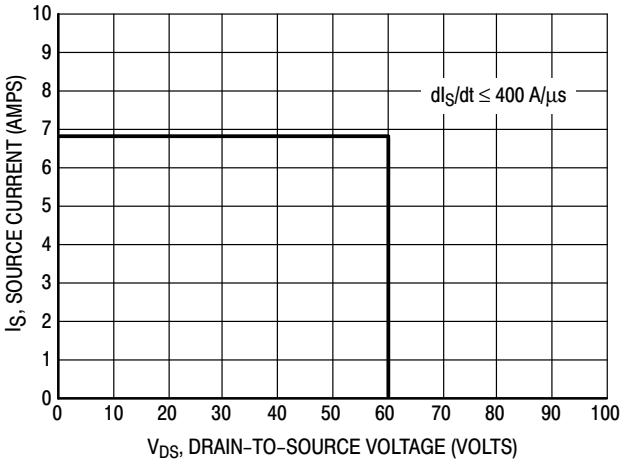


Figure 10. Commutating Safe Operating Area (CSOA)

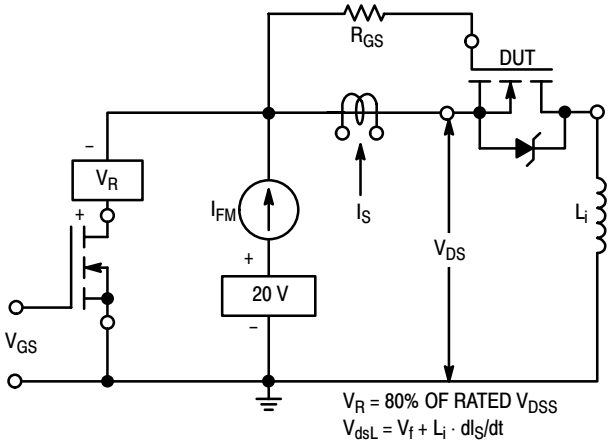


Figure 11. Commutating Safe Operating Area Test Circuit

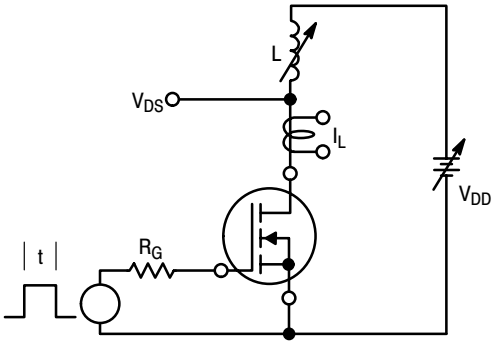


Figure 12. Unclamped Inductive Switching Test Circuit

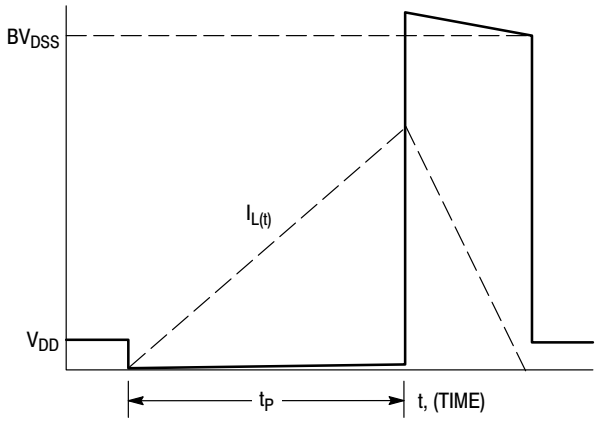


Figure 13. Unclamped Inductive Switching Waveforms

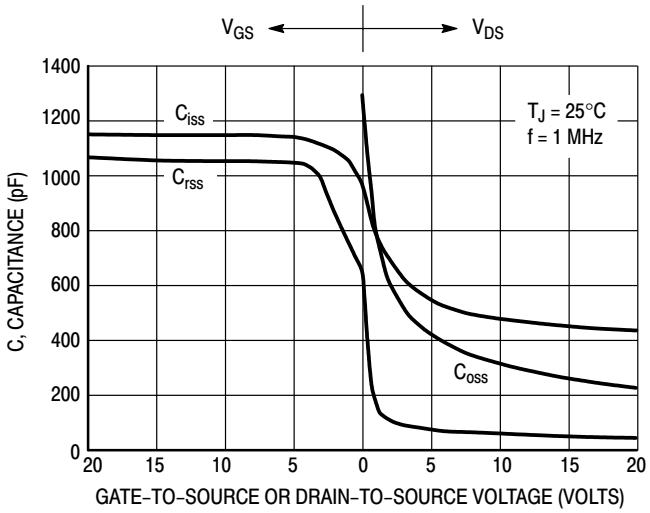


Figure 14. Capacitance Variation With Voltage

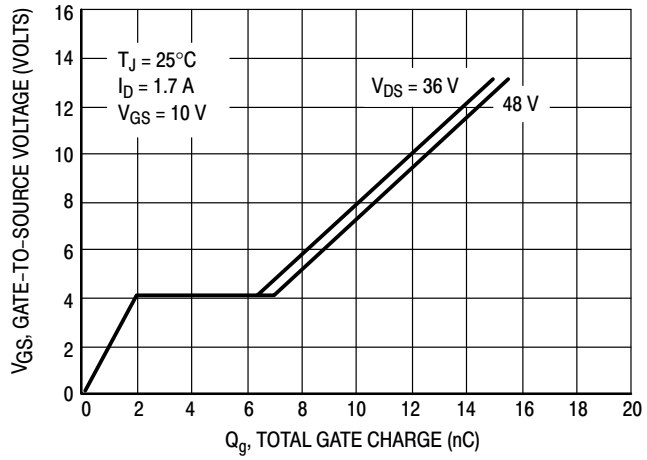
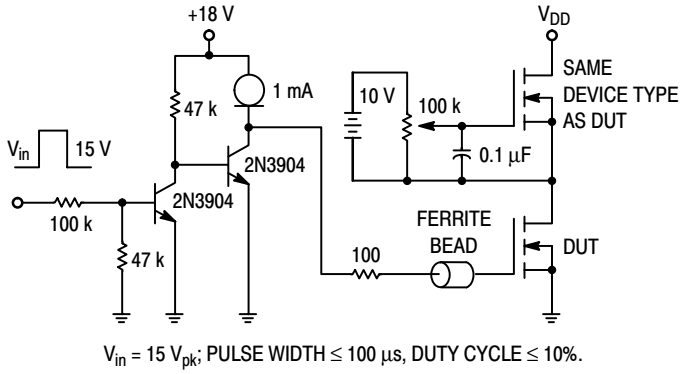


Figure 15. Gate Charge versus Gate−To−Source Voltage

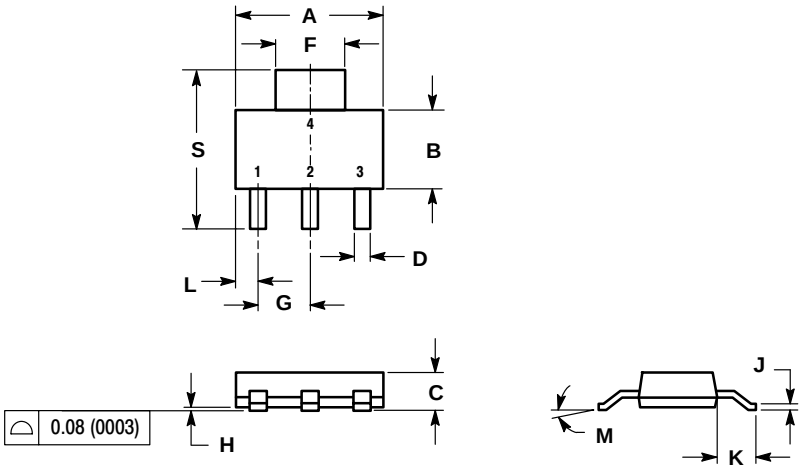


V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%.

Figure 16. Gate Charge Test Circuit

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE K

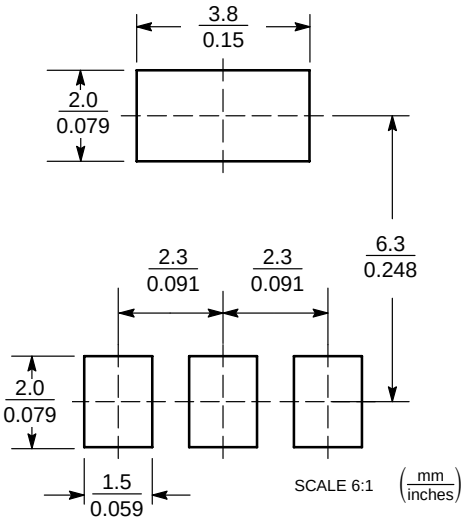


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PUBLICATION ORDERING INFORMATION

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