MITSUBISHI SEMICONDUCTOR <GaAs FET>

MGF4910D Series

TAPE CARRIER SUPER LOW NOISE InGaAs HEMT

DESCRIPTION

The MGF4910D series super-low-noise HEMT (High Electron Mobility Transistor) is designed for use in X to K band amplifiers. The hermetically sealed metal-ceramic package assures minimum parasitic losses, and has a configuration suitable for microstrip circuits. The MGF 4910D Series is mounted in the super 12 tape.

FEATURES

- Low noise figure @f=12GHz
  - MGF4914D: NFmin.=1.00dB (MAX)
  - MGF4916D: NFmin.=0.80dB (MAX)
  - MGF4917D: NFmin.=0.70dB (MAX)
  - MGF4918D: NFmin.=0.60dB (MAX)
- High associated gain Gs=9.5dB(MIN) @f=12GHz

APPLICATION

X to K band super-low-noise amplifiers.

QUALITY GRADE

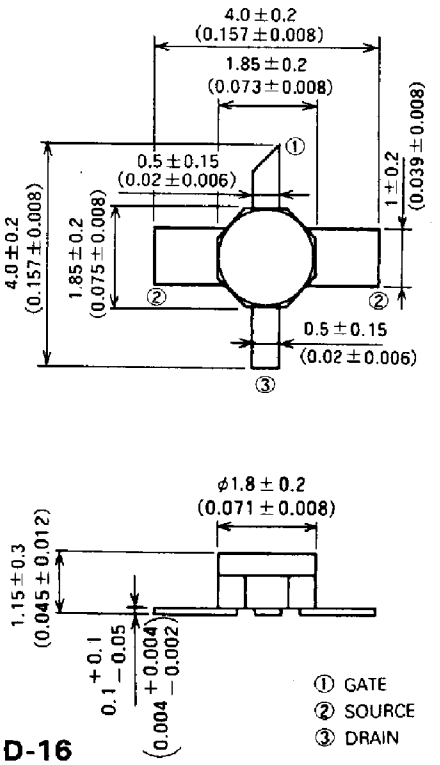
- GG

RECOMMENDED BIAS CONDITIONS

- V_{DS}=2V I_D=10mA
- Refer to Bias Procedure

OUTLINE DRAWING

Unit: millimeters (inches)



GD-16

ABSOLUTE MAXIMUM RATINGS (Ta=25℃)

Symbol	Parameter	Ratings	Unit
V_{GDO}	Gate to drain voltage	−4	V
V_{GSO}	Gate to source voltage	−4	V
I_D	Drain current	60	mA
P_T	Total power dissipation	50	mW
Tch	Channel temperature	125	℃
Tstg	Storage temperature	−65 − +125	℃

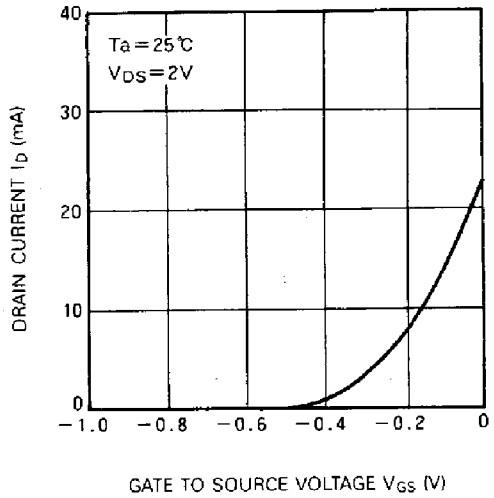
ELECTRICAL CHARACTERISTICS (Ta=25℃)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
$V_{(BR)GDO}$	Gate to drain breakdown voltage	I_G=−100μA		−3	—	—	V
$V_{(BR)GSO}$	Gate to source breakdown voltage	I_G=−100μA		−3	—	—	V
I_{GSS}	Gate to source leakage current	V_{GS}=−2V, V_{DS}=0V		—	—	50	μA
I_{DSS}	Saturated drain current	V_{GS}=0V, V_{DS}=2V		10	20	60	mA
$V_{GS(off)}$	Gate to source cut-off voltage	V_{DS}=2V, I_D=500μA		−0.1	—	−1.5	V
gm	Transconductance	V_{DS}=2V, I_D=10mA		40	60	—	mS
Gs	Associated gain	V_{DS}=2V, I_D=10mA, f=12GHz		9.5	11.5	—	dB
NFmin	Minimum noise figure		MGF4914D	—	—	1.00	dB
			MGF4916D	—	0.75	0.80	dB
			MGF4917D	—	0.65	0.70	dB
			MGF4918D	—	0.55	0.60	dB
Rth(ch-a)	Thermal resistance *1	$\triangle V_f$ method		—	—	625	℃/W

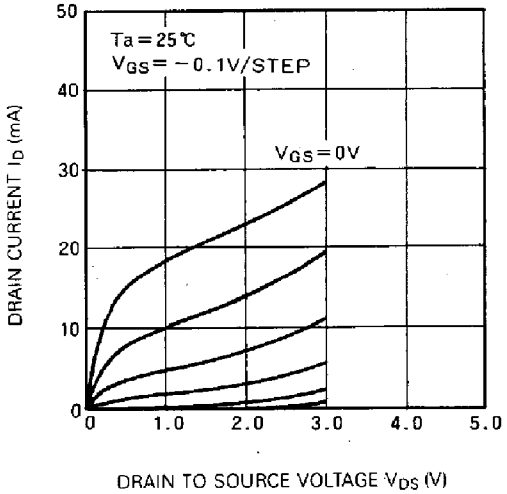
*1: Channel to ambient

TYPICAL CHARACTERISTICS (Ta=25℃)

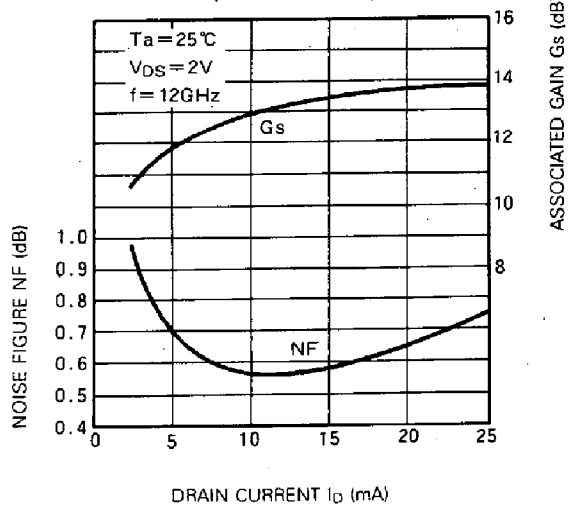
I_D vs. V_{GS}



I_D vs. V_{DS}



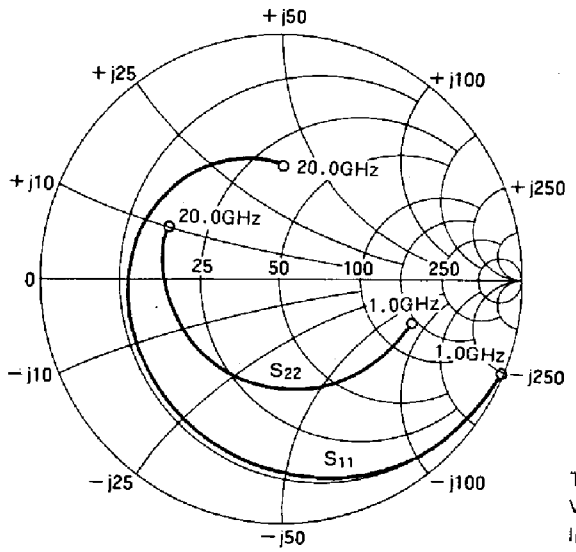
NF & Gs vs. I_D
(f=12GHz)
(MGF4918D)



MGF4910D Series

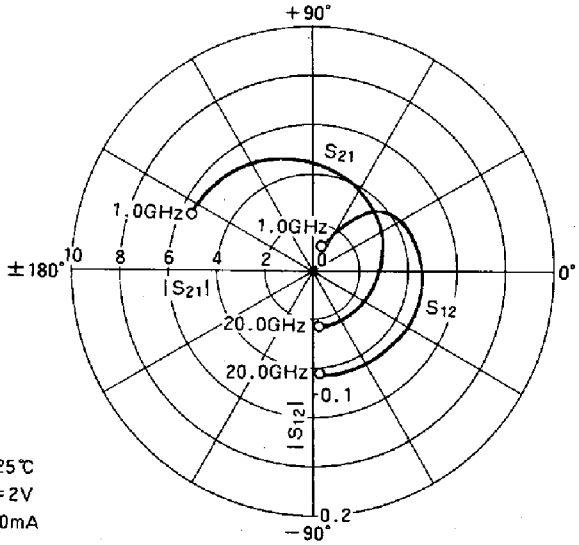
TAPE CARRIER SUPER LOW NOISE InGaAs HEMT

S_{11}, S_{22} vs. f.



Ta=25℃
V_{DS}=2V
I_D=10mA

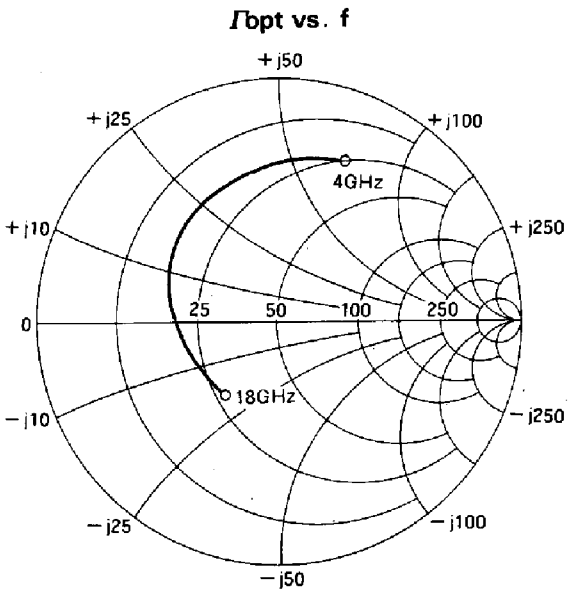
S_{21}, S_{12} vs. f.



S PARAMETERS (Ta=25℃, V_{DS}=2V, I_D=10mA)

Freq. (GHz)	S_{11}		S_{21}		S_{12}		S_{22}		K	MSG/MAG (dB)
	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.		
1.0	0.983	− 27.5	5.636	154.1	0.024	69.7	0.592	− 21.7	0.119	23.7
2.0	0.940	− 43.7	5.347	139.4	0.038	59.6	0.564	− 34.2	0.233	21.5
3.0	0.897	− 59.9	5.058	124.8	0.052	49.6	0.536	− 46.7	0.305	19.9
4.0	0.854	− 76.1	4.769	110.1	0.066	39.5	0.508	− 59.2	0.365	18.6
5.0	0.805	− 93.8	4.437	95.2	0.073	29.6	0.481	− 72.7	0.438	17.8
6.0	0.756	−111.4	4.105	80.3	0.081	19.7	0.453	− 86.1	0.520	17.0
7.0	0.726	−125.1	3.825	67.3	0.084	11.5	0.442	− 97.7	0.585	16.6
8.0	0.696	−138.8	3.545	54.3	0.087	3.3	0.431	−109.2	0.660	16.1
9.0	0.672	−151.1	3.337	42.6	0.088	− 3.3	0.433	−118.7	0.721	15.8
10.0	0.649	−163.3	3.129	30.8	0.089	− 9.8	0.436	−128.1	0.790	15.5
11.0	0.633	−175.6	2.984	19.1	0.089	−16.9	0.435	−137.2	0.852	15.3
12.0	0.618	172.2	2.839	7.4	0.089	−23.9	0.434	−146.2	0.921	15.0
13.0	0.608	162.9	2.722	− 3.1	0.087	−28.5	0.450	−154.4	0.974	15.0
14.0	0.599	153.5	2.605	−13.6	0.084	−33.0	0.467	−162.5	1.033	13.8
15.0	0.582	143.6	2.536	−24.7	0.085	−39.9	0.484	−169.6	1.061	13.2
16.0	0.566	133.7	2.468	−35.8	0.086	−46.8	0.501	−176.7	1.087	12.8
17.0	0.545	122.0	2.439	−48.2	0.089	−56.1	0.515	175.9	1.095	12.5
18.0	0.525	110.3	2.410	−60.5	0.091	−65.3	0.529	168.4	1.101	12.3
19.0	0.495	99.2	2.363	−73.1	0.090	−76.0	0.523	161.9	1.229	11.3
20.0	0.465	88.1	2.315	−85.6	0.089	−86.6	0.518	155.4	1.359	10.6

NOISE PARAMETERS



Ta = 25℃
V_{DS} = 2V
I_D = 10mA

f	Γopt		Rn	NFmin (dB)				Gs
(GHz)	Magn.	Angle (deg.)	(Ω)	MGF4914D	MGF4916D	MGF4917D	MGF4918D	(dB)
4	0.72	65	13.5	0.41	0.36	0.31	0.29	16.5
8	0.57	125	5.5	0.62	0.56	0.49	0.43	12.8
12	0.45	165	1.9	0.90	0.75	0.65	0.55	11.5
14	0.41	−173	1.7	1.03	0.85	0.74	0.63	10.0
18	0.36	−125	1.6	1.29	1.04	0.92	0.80	7.4

FUNCTION

Read

Set the $\overline{CE}$ and $\overline{OE}$ terminals to the read mode (low level). Low level input to $\overline{CE}$ and $\overline{OE}$ and address signals to the address inputs ($A_0 \sim A_{15}$) make the data contents of the designated address location available at the data input/output ($D_0 \sim D_{15}$). When the $\overline{CE}$ or $\overline{OE}$ signal is high, data input/output are in a floating state.

When the $\overline{CE}$ signal is high, the device is in the standby mode or power-down mode.

Programming

(Word programming algorithm)

The M5M27C102P, FP, J, VP, RV-15 enter the word programming mode when 12.5V is supplied to the V_{PP} power supply input, $\overline{CE}$ is at low level and $\overline{OE}$ is at high level. A location is designated by address signals ($A_0 \sim A_{15}$), and the data to be programmed must be applied at 16-bits in parallel to the data inputs ($D_0 \sim D_{15}$). In this state, word programming is completed when $\overline{PGM}$ is at low level.

(Page programming algorithm)

Page programming feature of the M5M27C102P, FP, J, VP, RV-15 allows 2 words of data to be simultaneously programmed. The destination addresses for a page programming operation must reside on the same page; that is, A_1 through A_{15} must not change. At first, the M5M27C102P, FP, J, VP, RV-15 enter the page data latch mode when V_{PP} = 12.5V, $\overline{CE}$ = "H", $\overline{OE}$ = "L" and $\overline{PGM}$ = "H". A first and second locations in same page are designated by address signals ($A_0 \sim A_{15}$), and the data to be programmed must be applied to each location at 16-bits in parallel to the data inputs ($D_0 \sim D_{15}$). In this state, the data (2 words) latch is completed. Then the M5M27C102P, FP, J, VP, RV-15 enter the page programming mode when $\overline{OE}$ = "H". In this state, page (2 words) programming is completed when $\overline{PGM}$ = "L".

Erase

The M5M27C102P, FP, J, VP, RV-15 cannot be erased, because they are packaged in plastic without transparent lid.

MODE SELECTION

Mode \ Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read	V_{IL}	V_{IL}	X*	5V	5V	Data out
Output disable	V_{IL}	V_{IH}	X*	5V	5V	Floating
Standby (Power down)	V_{IH}	X*	X*	5V	5V	Floating
Word program	V_{IL}	V_{IH}	V_{IL}	12.5V	6V	Data in
Program verify	V_{IL}	V_{IL}	V_{IH}	12.5V	6V	Data out
Page data latch	V_{IH}	V_{IL}	V_{IH}	12.5V	6V	Data in
Page program	V_{IH}	V_{IH}	V_{IL}	12.5V	6V	Floating
Program inhibit	V_{IL}	V_{IL}	V_{IL}	12.5V	6V	Floating
	V_{IL}	V_{IH}	V_{IH}	12.5V	6V	
	V_{IH}	V_{IL}	V_{IL}	12.5V	6V	
	V_{IH}	V_{IH}	V_{IH}	12.5V	6V	

*: X can be either V_{IL} or V_{IH}.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Test condition	Ratings	Unit
V_{I1}	All input or output voltage except V_{PP}·A_9	With respect to Ground	−0.6~7	V
V_{I2}	V_{PP} supply voltage		−0.6~14.0	V
V_{I3}	A_9 supply voltage		−0.6~13.5	V
Topr	Operating temperature		−10~80	°C
Tstg	Storage temperature		−65~150	°C

Note 1: Stresses above those listed may cause parmanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

READ OPERATION

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input load current	V_{IN}=0V~V_{CC}			10	μA
I_{LO}	Output leakage current	V_{OUT}=0V~V_{CC}			10	μA
I_{PP1}	V_{PP} current read	V_{PP}=5.5V		1	100	μA
I_{SB1}	V_{CC} current standby	$\overline{CE}$=V_{IH}			1	mA
I_{SB2}		$\overline{CE}$=V_{CC}		1	100	μA
I_{CC1}	V_{CC} current Active	$\overline{OE}$=$\overline{OE}$=V_{IL}			50	mA
I_{CC2}		f=6.7MHz, I_{OUT}=0mA			50	mA
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V

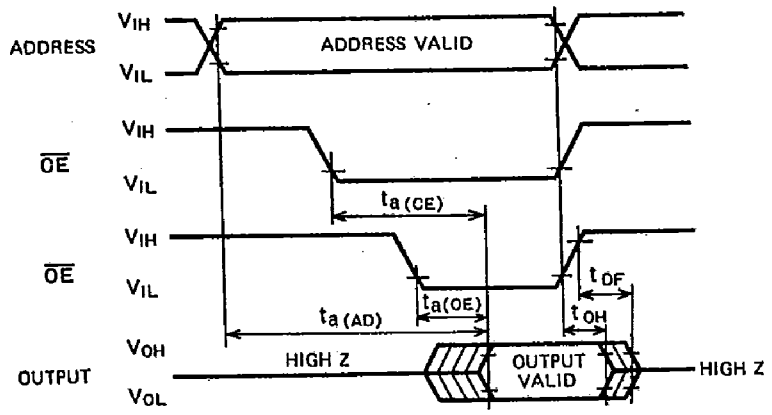
Note 2: Typical values are at T_a = 25°C and nominal supply voltages.

AC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%, V_{PP}=V_{CC}, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(AD)}$	Address to output delay	$\overline{CE}$=$\overline{OE}$=V_{IL}			150	ns
$t_{a(\overline{CE})}$	$\overline{CE}$ to output delay	$\overline{OE}$=V_{IL}			150	ns
$t_{a(\overline{OE})}$	Output enable to output delay	$\overline{OE}$=V_{IL}			60	ns
t_{DF}	Output enable high to output float	$\overline{OE}$=V_{IL}	0		50	ns
t_{OH}	Output hold from $\overline{CE}$, $\overline{OE}$ or addresses		0			ns

Note 3: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

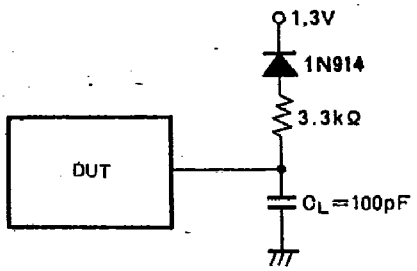
AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input, Output "L" = 0.8V, "H" = 2V.

Output load: 1TTL gate + C_L (100pF)

or



CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_{IN}	Input capacitance (Address, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	T_a=25°C, f=1MHz, V_I=V_O=0V			15	pF
C_{OUT}	Output capacitance				15	pF

WORD PROGRAMMING ALGORITHM

First set V_{CC} = 6V, V_{PP} = 12.5V and then set an address to first address to be programmed. After applying 0.2 ms program pulse ($\overline{PGM}$) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 0.2 ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with $V_{CC} = V_{PP} = 5V$.

DC ELECTRICAL CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

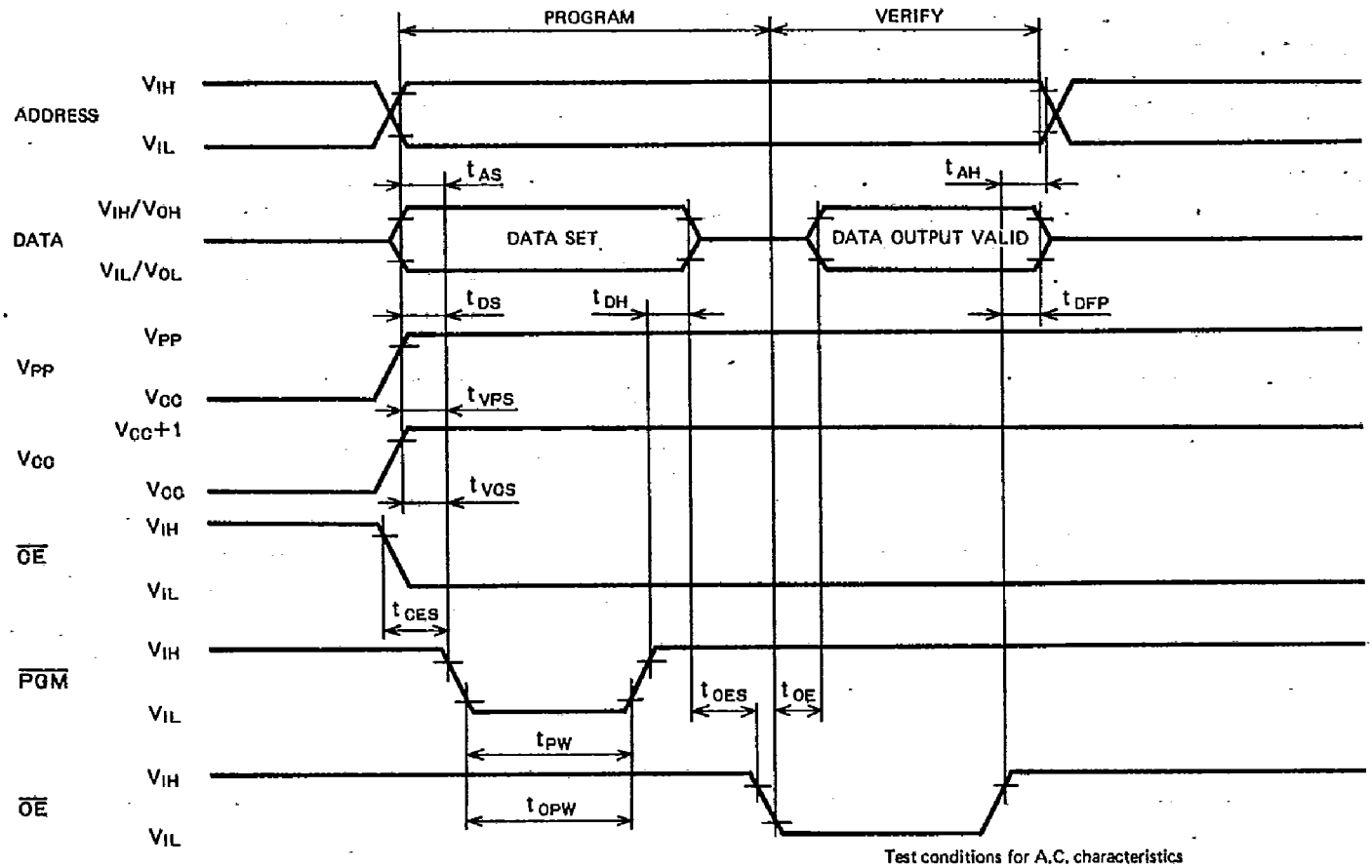
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	V_{IN}=0V~V_{CC}			10	μA
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CC}	V_{CC} supply current				50	mA
I_{PP}	V_{PP} supply current	$\overline{CE}$=$\overline{PGM}$=V_{IL}			50	mA

AC ELECTRICAL CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ set up time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Chip enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

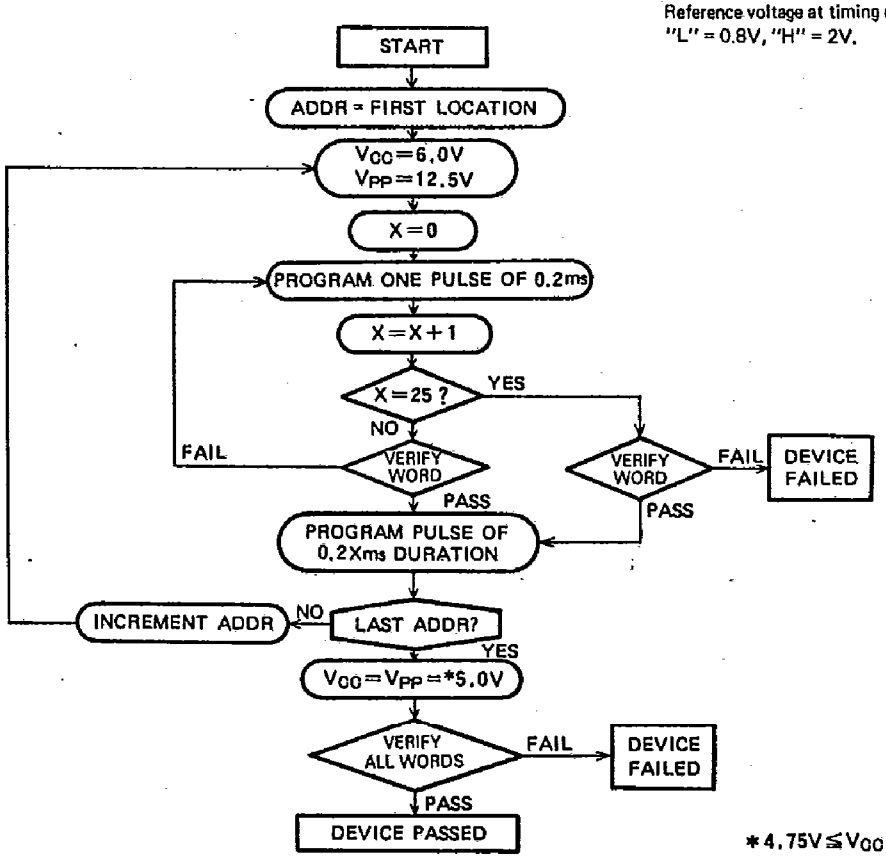
Note 4: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

AC WAVEFORMS



Test conditions for A.C. characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall times: ≦ 20ns
Reference voltage at timing measurement: Input, Output "L" = 0.8V, "H" = 2V.

WORD PROGRAMMING ALGORITHM FLOW CHART



*4.75V≦VCC=VPP≦5.25V

PAGE PROGRAMMING ALGORITHM

First set V_{CC} = 6V, V_{PP} = 12.5V and then set an address to first page address to be programmed. After data of 2 words are latched, these latch data are programmed simultaneously by applying 0.2 ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also maintains its total number of 0.2 ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with V_{CC} = V_{PP} = 5V.

DC ELECTRICAL CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

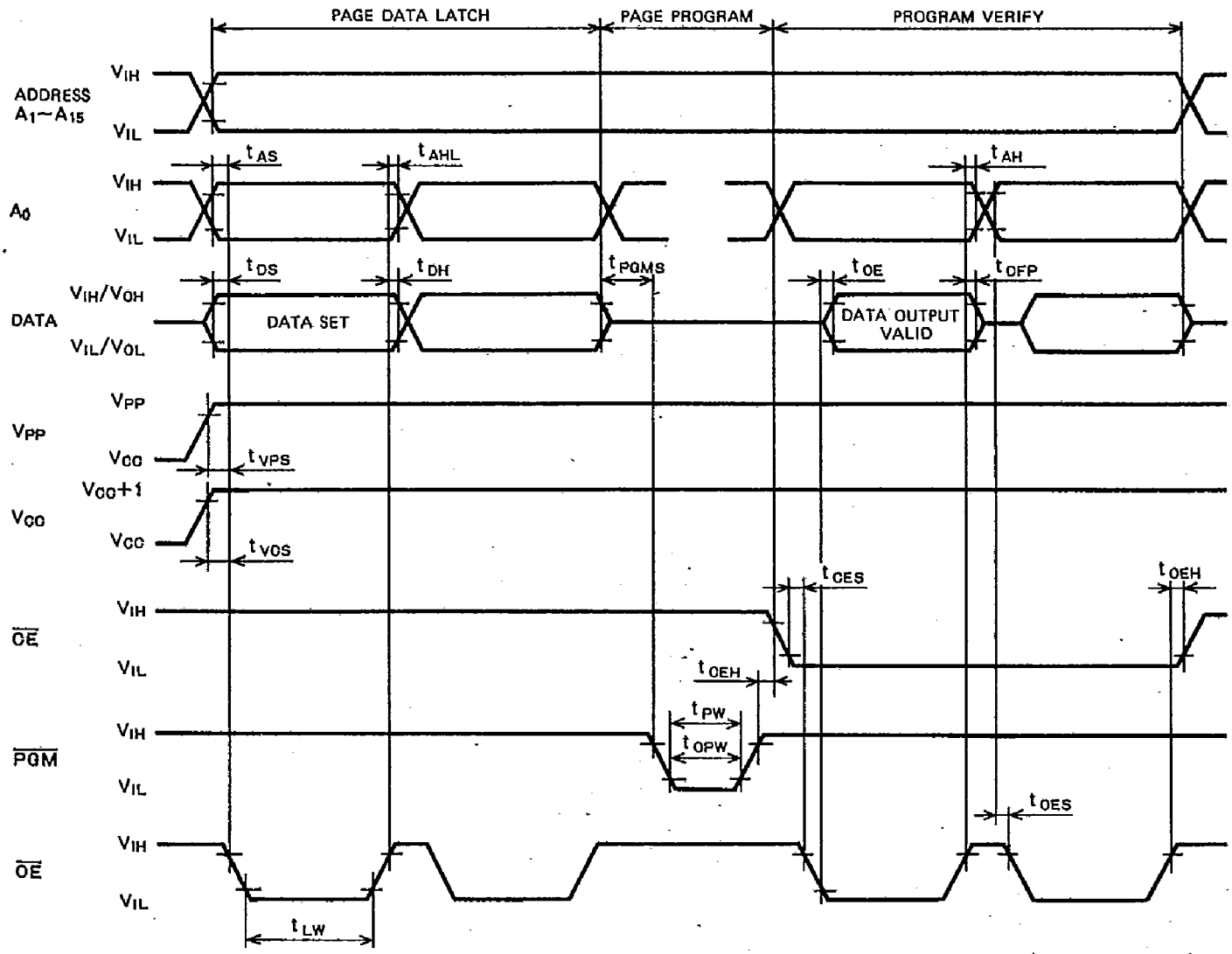
Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
I_{LI}	Input current	V_{IN}=0V~V_{CC}			10	μA
V_{OL}	Output low voltage	I_{OL}=2.1mA			0.45	V
V_{OH}	Output high voltage	I_{OH}=−400μA	2.4			V
V_{IL}	Input low voltage		−0.1		0.8	V
V_{IH}	Input high voltage		2.0		V_{CC}	V
I_{CO}	V_{CC} supply current				50	mA
I_{PP}	V_{PP} supply current	$\overline{PGM}$=V_{IL}			100	mA

AC ELECTRICAL CHARACTERISTICS (T_a=25±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{AHL}			2			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	$\overline{OE}$ to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ initial program pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns
t_{LW}	Data latch time		1			μs
t_{PGMS}	$\overline{PGM}$ setup time		2			μs
t_{CEH}	$\overline{CE}$ hold time		2			μs
t_{OEH}	$\overline{OE}$ hold time		2			μs

Note 5: V_{CC} must be applied simultaneously V_{PP} and removed simultaneously V_{PP}.

AC WAVEFORMS



Test condition for A.C characteristics
Input voltage: V_{IL} = 0.45V, V_{IH} = 2.4V
Input rise and fall time: (10% ~ 90%): ≦ 20ns
Reference voltage at timing measurement: Input, Output "L" = 0.8V, "H" = 2V.