

DATA SHEET

BSP92

P-channel enhancement mode
vertical D-MOS transistor

Product specification
File under Discrete Semiconductors, SC13b

April 1995

P-channel enhancement mode vertical D-MOS transistor

BSP92

FEATURES

- Low threshold voltage $V_{GS(th)}$
- Direct interface to C-MOS, TTL, etc.
- High-speed switching
- No secondary breakdown.

DESCRIPTION

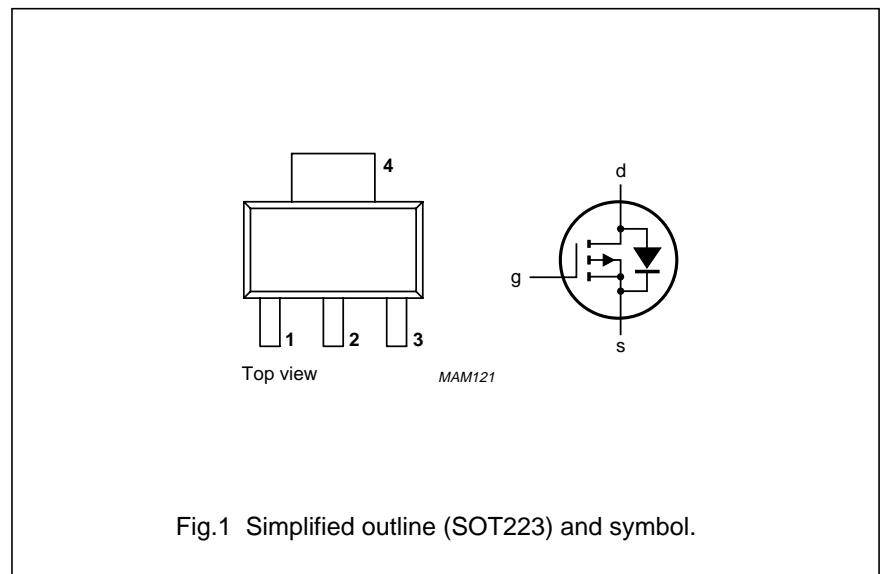
P-channel enhancement mode vertical D-MOS transistor in a SOT223 envelope, intended for use as a surface-mounted device in line current interruptor in telephone sets and for application in relay, high speed and line transformer drivers.

PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$-V_{DS}$	drain-source voltage	240	V
$-I_D$	DC drain current	180	mA
$R_{DS(on)}$	drain-source on-resistance	20	Ω
$-V_{GS(th)}$	gate-source threshold voltage	1.8	V



LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$-V_{DS}$	drain-source voltage		–	240	V
$\pm V_{GSO}$	gate-source voltage	open drain	–	20	V
$-I_D$	DC drain current		–	180	mA
$-I_{DM}$	peak drain current		–	720	mA
P_{tot}	total power dissipation	up to $T_{amb} = 25\text{ }^\circ\text{C}$ (note 1)	–	1.5	W
T_{stg}	storage temperature range		–65	150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j-a}$	from junction to ambient (note 1)	83.3 K/W

Note

1. Transistor mounted on an epoxy printed circuit board, 40 x 40 x 1.5 mm, mounting pad for the drain tab minimum 6 cm².

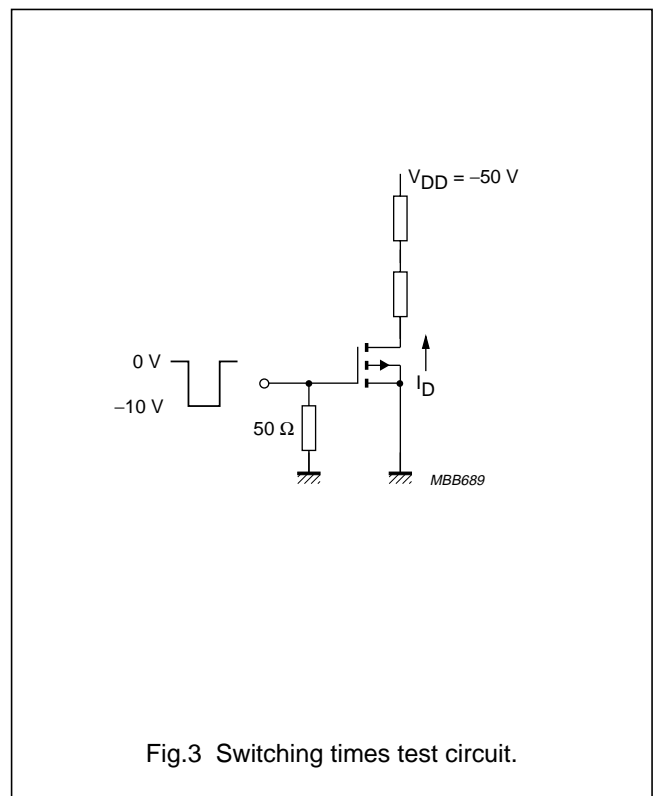
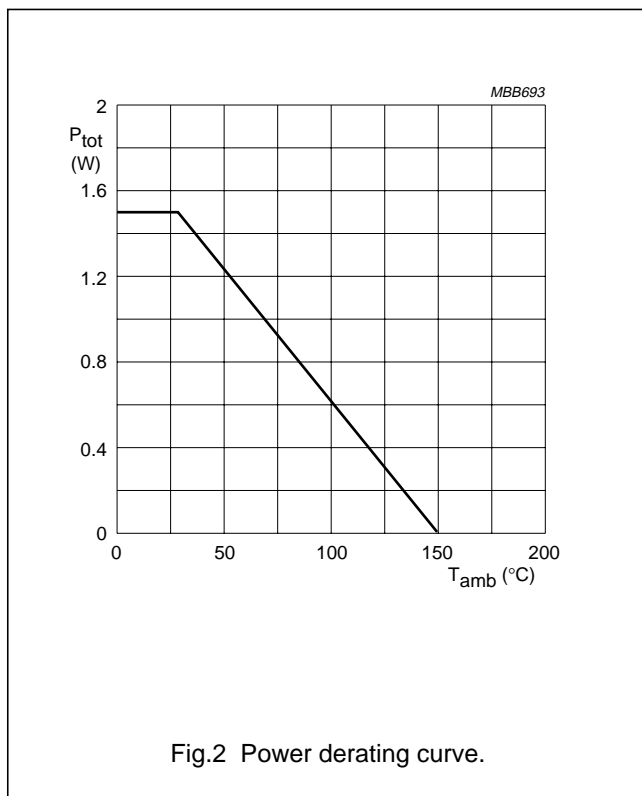
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CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$-V_{(BR)DSS}$	drain-source breakdown voltage	$-I_D = 10\text{ }\mu\text{A}; V_{GS} = 0$	240	–	–	V
$-I_{DSS}$	drain-source leakage current	$-V_{DS} = 200\text{ V}; V_{GS} = 0$	–	–	1	μA
$\pm I_{GSS}$	gate-source leakage current	$\pm V_{GS} = 20\text{ V}; V_{DS} = 0$	–	–	100	nA
$-V_{GS(th)}$	gate-source threshold voltage	$-I_D = 1\text{ mA}; V_{GS} = V_{DS}$	0.8	–	2	V
$-V_{GS}$	gate-source voltage	$-I_D = 50\text{ mA}; -V_{DS} = 5\text{ V}$	0.8	–	2.8	V
$R_{DS(on)}$	drain-source on-resistance	$-I_D = 180\text{ mA}; -V_{GS} = 10\text{ V}$	–	10	20	Ω
		$-I_D = 100\text{ mA}; -V_{GS} = 5\text{ V}$	–	–	18	Ω
		$-I_D = 25\text{ mA}; -V_{GS} = 2.8\text{ V}$	–	–	20	Ω
$ Y_{fs} $	transfer admittance	$-I_D = 180\text{ mA}; -V_{DS} = 25\text{ V}$	100	200	–	mS
C_{iss}	input capacitance	$-V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	65	90	pF
C_{oss}	output capacitance	$-V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	20	30	pF
C_{rss}	feedback capacitance	$-V_{DS} = 25\text{ V}; V_{GS} = 0; f = 1\text{ MHz}$	–	6	15	pF
Switching times (see Figs 3 and 4)						
t_{on}	turn-on time	$-I_D = 250\text{ mA}; -V_{DD} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	–	5	10	ns
t_{off}	turn-off time	$-I_D = 250\text{ mA}; -V_{DD} = 50\text{ V}; -V_{GS} = 0\text{ to }10\text{ V}$	–	20	30	ns



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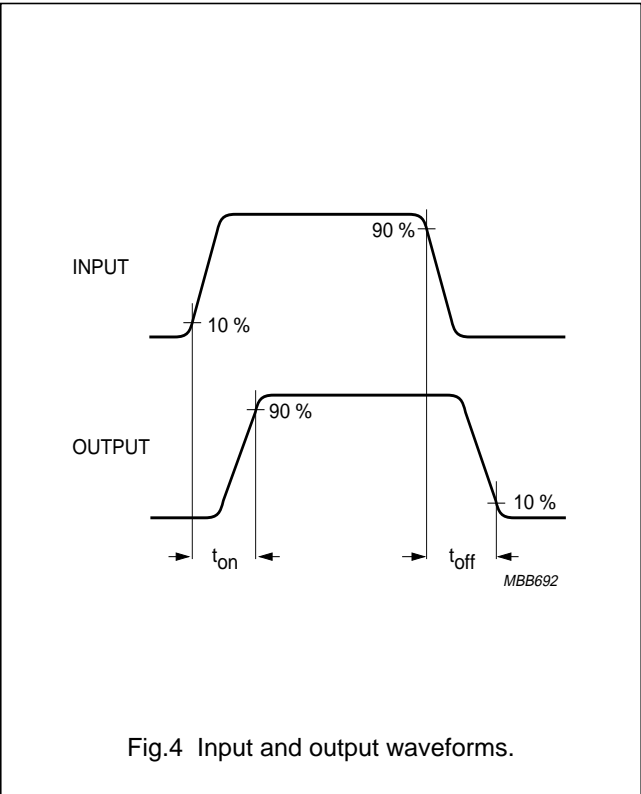


Fig.4 Input and output waveforms.

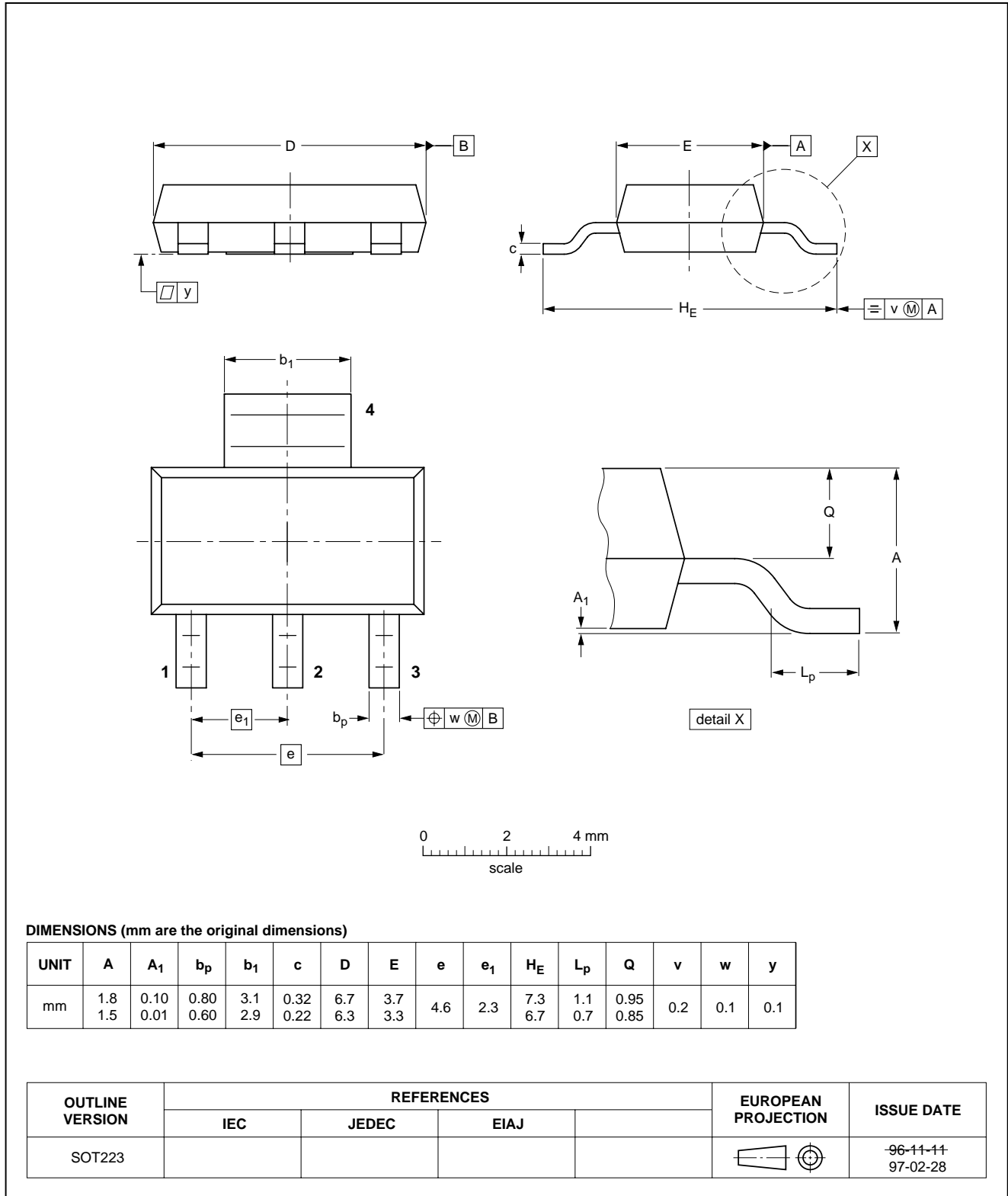
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PACKAGE OUTLINES

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



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BSP92**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Printed in The Netherlands

137107/00/01/pp8

Date of release: April 1995

Document order number: 9397 750 02486

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