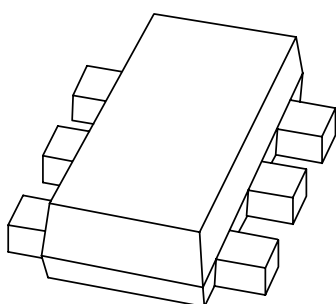


DATA SHEET



PEMX1 NPN general purpose double transistor

Product specification
Supersedes data of 2001 Aug 30

2001 Nov 07

NPN general purpose double transistor

PEMX1

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm x 1.2 mm ultra thin package
- Excellent coplanarity due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduced required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification.

DESCRIPTION

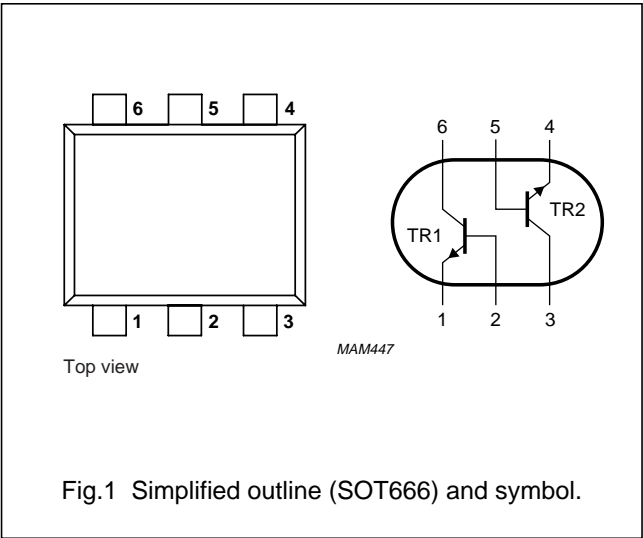
NPN double transistor pair in a SOT666 plastic package.
PNP complement: PENT1.

MARKING

TYPE NUMBER	MARKING CODE
PEMX1	ZZ

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	40	V
V _{EBO}	emitter-base voltage	open collector	–	5	V
I _C	collector current (DC)		–	100	mA
I _{CM}	peak collector current		–	200	mA
I _{BM}	peak base current		–	200	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Note

1. Transistor mounted on an FR4 printed-circuit board.

NPN general purpose double transistor

PEMX1

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering is reflow soldering.

CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
I_{CBO}	collector-base cut-off current	$V_{CB} = 30\text{ V}; I_E = 0$	–	100	nA
		$V_{CB} = 30\text{ V}; I_E = 0; T_j = 150\text{ °C}$	–	10	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 4\text{ V}; I_C = 0$	–	100	nA
h_{FE}	DC current gain	$V_{CE} = 6\text{ V}; I_C = 1\text{ mA}$	120	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\text{ mA}; I_B = 5\text{ mA}; \text{note 1}$	–	200	mV
C_c	collector capacitance	$V_{CB} = 12\text{ V}; I_E = I_e = 0; f = 1\text{ MHz}$	–	1.5	pF
f_T	transition frequency	$I_C = 2\text{ mA}; V_{CE} = 12\text{ V}; f = 100\text{ MHz}$	100	–	MHz

Note

1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

NPN general purpose double transistor

PEMX1

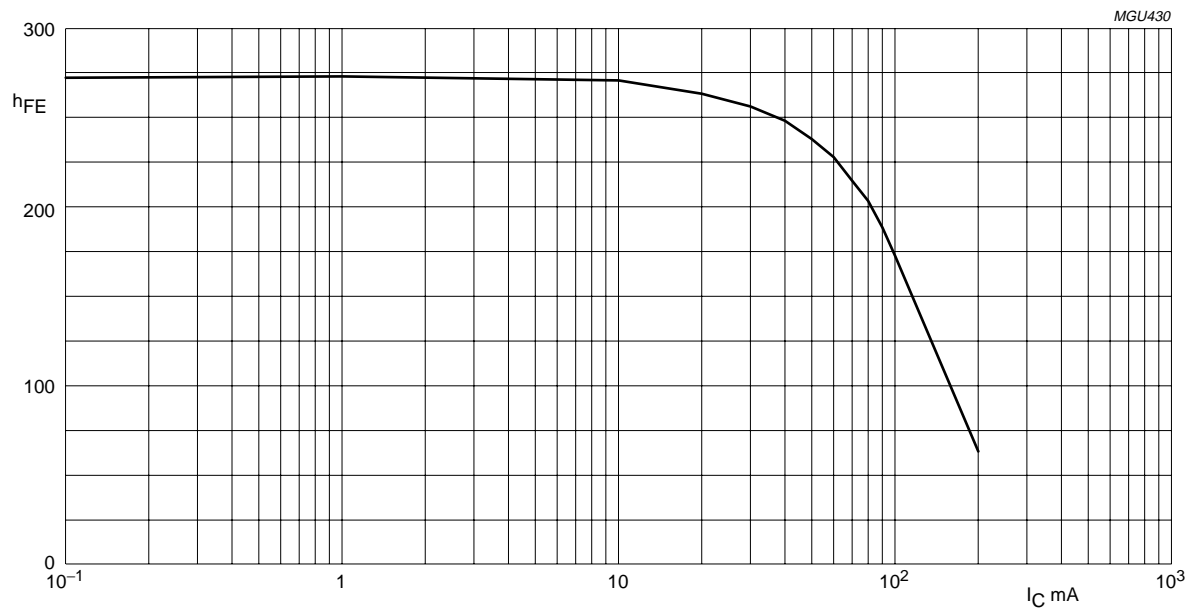


Fig.2 DC current gain as a function of collector current; typical values.

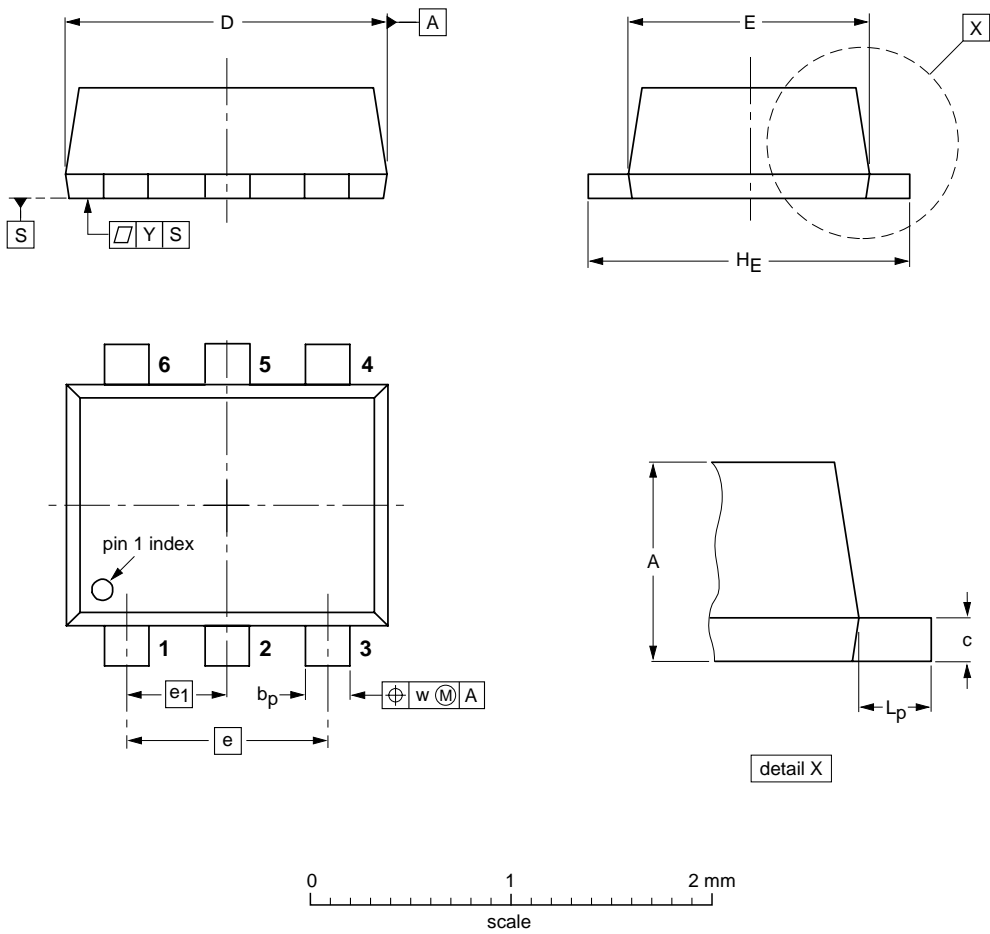
NPN general purpose double transistor

PEMX1

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _p	c	D	E	e	e ₁	H _E	L _p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

NPN general purpose double transistor

PEMX1

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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PEMX1

NOTES

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