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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT1059C

Silicon P Channel Power MOS FET Power Switching

RENESAS

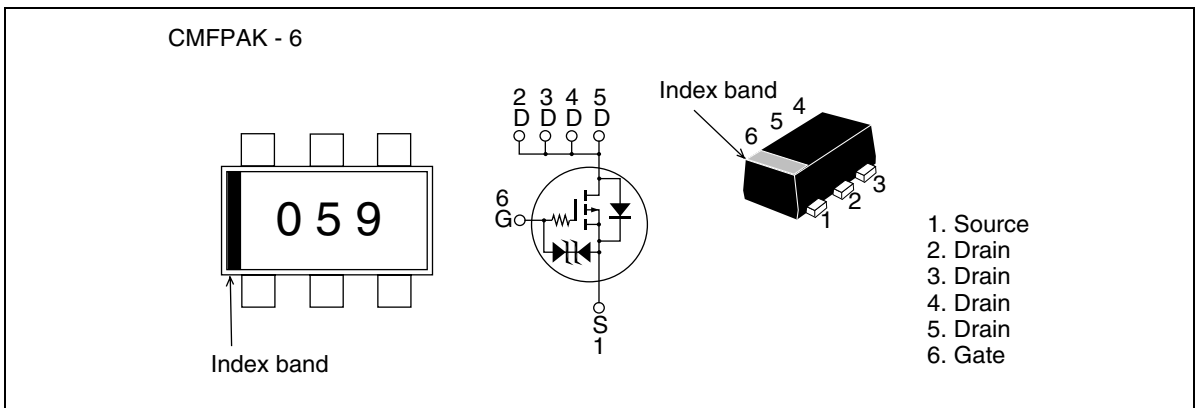
ADE-208-1450A (Z)

Rev.1
Sep. 2001

Features

- Low on-resistance
 $R_{DS(on)} = 52 \text{ m}\Omega$ typ (at $V_{GS} = -4.5 \text{ V}$, $I_D = -1.5 \text{ A}$)
 $R_{DS(on)} = 71 \text{ m}\Omega$ typ (at $V_{GS} = -2.5 \text{ V}$, $I_D = -1.5 \text{ A}$)
 $R_{DS(on)} = 98 \text{ m}\Omega$ typ (at $V_{GS} = -1.8 \text{ V}$, $I_D = -1.5 \text{ A}$)
- Capable of 1.8 V gate drive
- Small Package: CMFPAK-6

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	-12	V
Gate to source voltage	V_{GSS}	±8	V
Drain current	I_D	-3	A
Channel dissipation	Pch	0.65	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

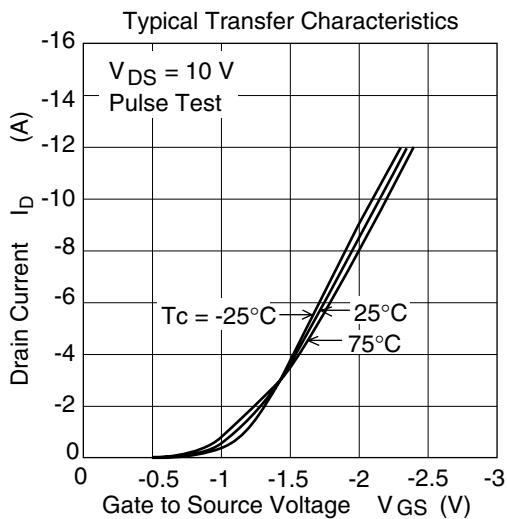
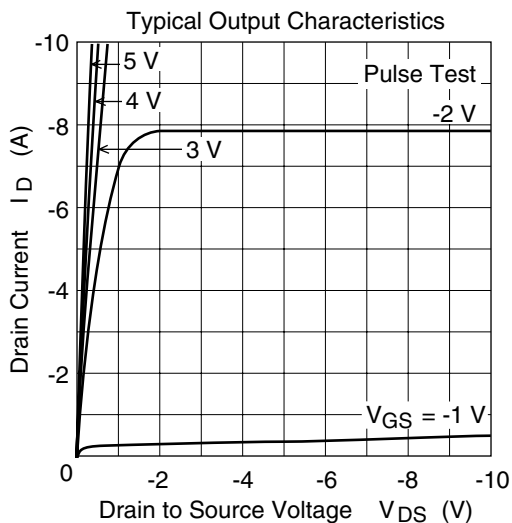
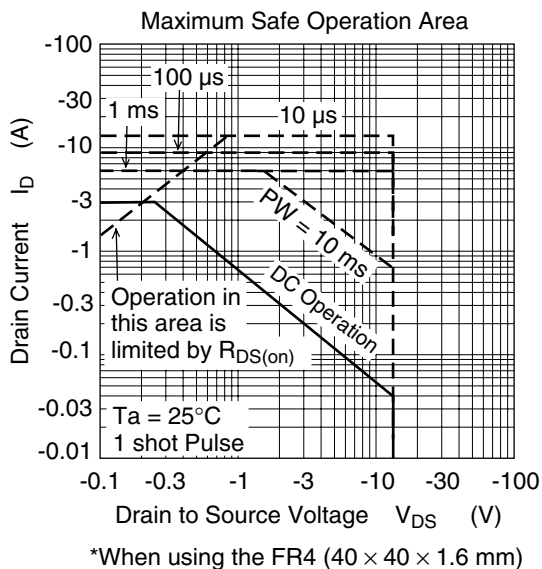
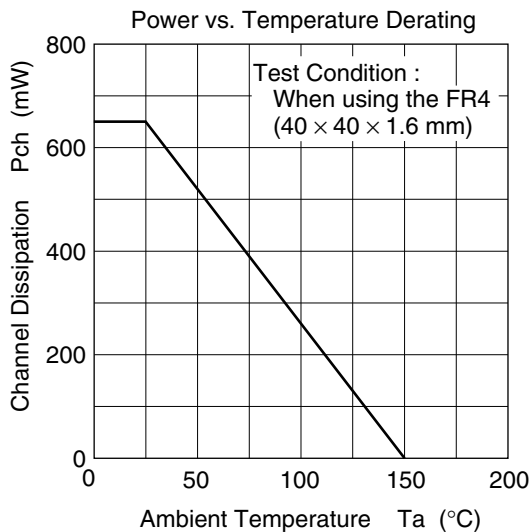
*Value on the FR4. (40 × 40 × 1.6 mm)

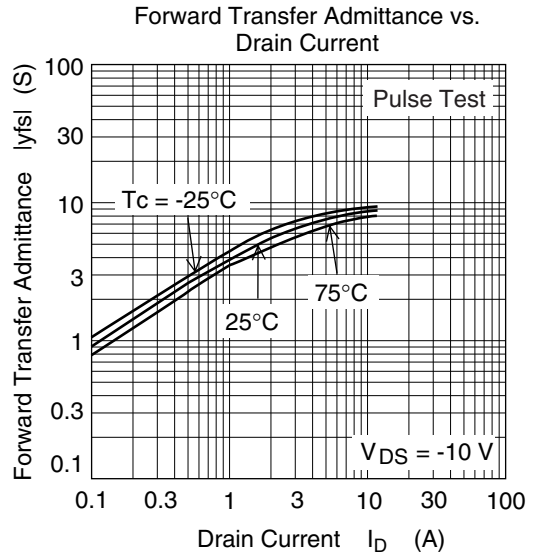
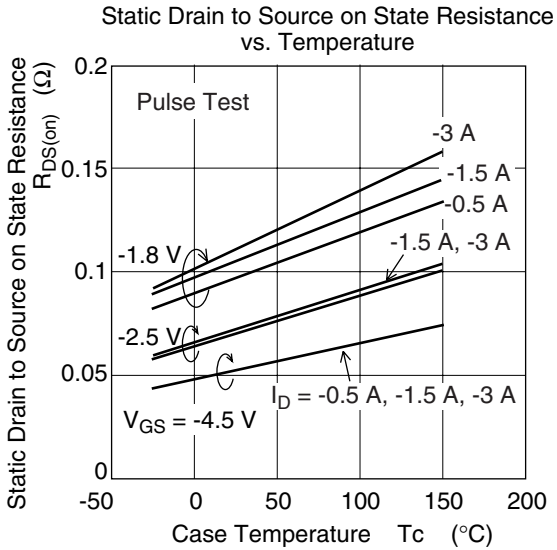
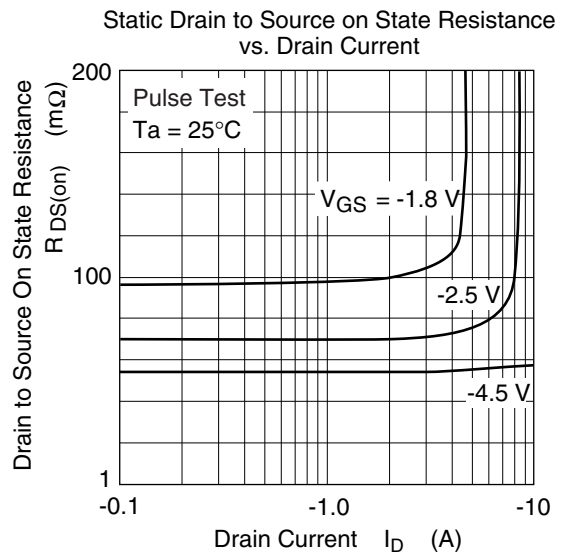
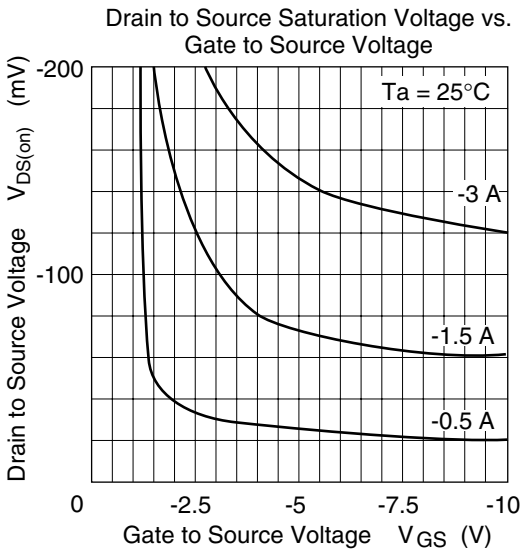
Electrical Characteristics

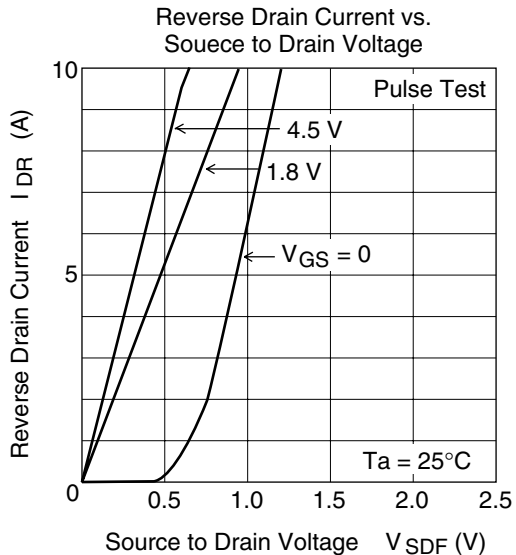
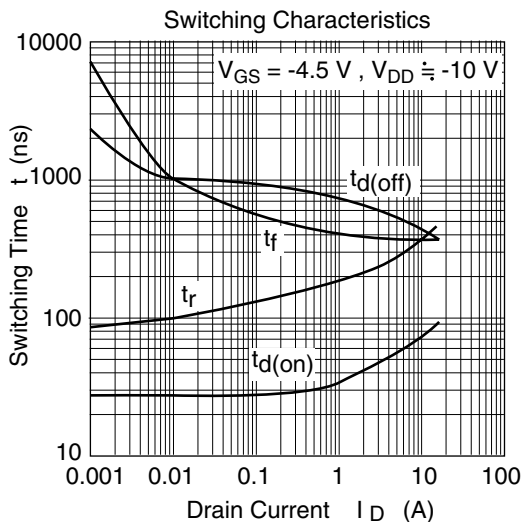
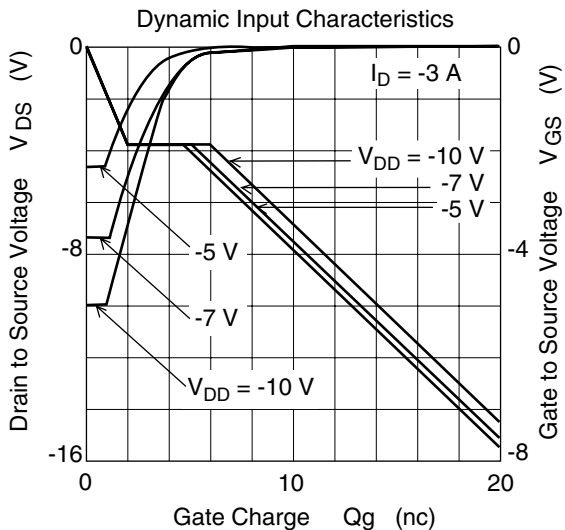
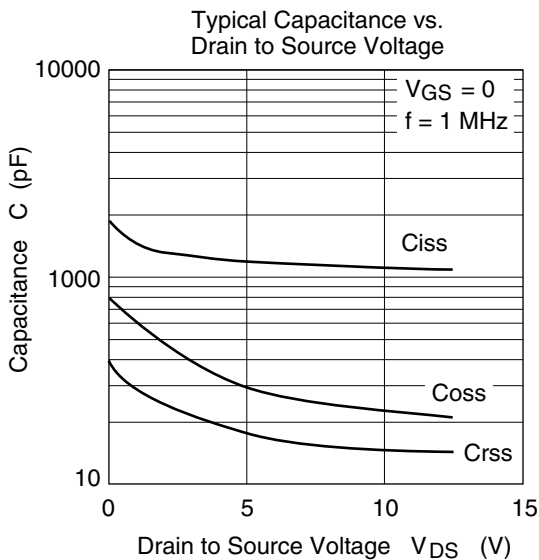
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-12	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±8	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 6.4 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -12 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-0.2	—	-1.0	V	$I_D = -1 \text{ mA}$, $V_{DS} = -10 \text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	52	64	mΩ	$I_D = -1.5 \text{ A}$, $V_{GS} = -4.5 \text{ V}$
	$R_{DS(on)}$	—	71	88	mΩ	$I_D = -1.5 \text{ A}$, $V_{GS} = -2.5 \text{ V}$
	$R_{DS(on)}$	—	98	126	mΩ	$I_D = -1.5 \text{ A}$, $V_{GS} = -1.8 \text{ V}$
Forward transfer admittance	$ y_{fs} $	4	5	—	S	$I_D = -1.5 \text{ A}$, $V_{DS} = -10 \text{ V}$
Input capacitance	Ciss	—	1080	—	pF	$V_{DS} = -10 \text{ V}$
Output capacitance	Coss	—	215	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	150	—	pF	f = 1 MHz
Total gate charge	Qg	—	13	—	nC	$V_{DS} = -10 \text{ V}$
Gate to source charge	Qgs	—	2.2	—	nC	$V_{GS} = -4.5 \text{ V}$
Gate to drain charge	Qdg	—	3.8	—	nC	$I_D = -3 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	35	—	ns	$V_{GS} = -4 \text{ V}$, $I_D = -1.5 \text{ A}$
Rise time	t_r	—	170	—	ns	$R_L = 6.66 \text{ } \Omega$
Turn-off delay time	$t_{d(off)}$	—	690	—	ns	
Fall time	t_f	—	460	—	ns	
Body-drain diode forward voltage	V_{SDF}	—	-0.85	-1.20	V	$I_F = -3.0 \text{ A}$, $V_{GS} = 0$

Main Characteristics

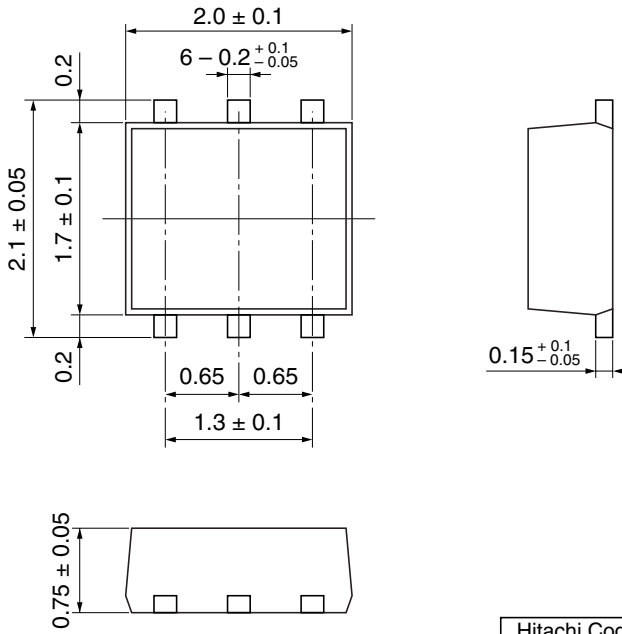






Package Dimensions

Unit: mm



Hitachi Code	CMFPAK-6
JEDEC	—
JEITA	Conforms
Mass (reference value)	1.2 mg

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