

# BCW72LT1G

## General Purpose Transistor NPN Silicon

### Features

- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage	$V_{CEO}$	45	Vdc
Collector - Base Voltage	$V_{CBO}$	50	Vdc
Emitter - Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current - Continuous	$I_C$	100	mAdc

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board, (Note 1) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	225 1.8	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	$^\circ\text{C}/\text{W}$
Total Device Dissipation Alumina Substrate, (Note 2) $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	300 2.4	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

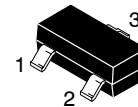
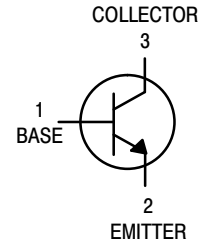
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR-5 = 1.0 x 0.75 x 0.062 in.
2. Alumina = 0.4 x 0.3 x 0.024 in. 99.5% alumina.



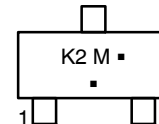
ON Semiconductor®

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SOT-23 (TO-236)  
CASE 318  
STYLE 6

### MARKING DIAGRAM



K2 = Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or overbar may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping†
BCW72LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# BCW72LT1G

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector – Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA <sub>dc</sub> , V <sub>EB</sub> = 0)	V <sub>(BR)CEO</sub>	45	–	–	V <sub>dc</sub>
Collector – Emitter Breakdown Voltage (I <sub>C</sub> = 2.0 mA <sub>dc</sub> , V <sub>EB</sub> = 0)	V <sub>(BR)CES</sub>	45	–	–	V <sub>dc</sub>
Collector – Base Breakdown Voltage (I <sub>C</sub> = 10 μA <sub>dc</sub> , I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	V <sub>dc</sub>
Emitter – Base Breakdown Voltage (I <sub>E</sub> = 10 μA <sub>dc</sub> , I <sub>C</sub> = 0)	V <sub>(BR)EBO</sub>	5.0	–	–	V <sub>dc</sub>
Collector Cutoff Current (V <sub>CB</sub> = 20 V <sub>dc</sub> , I <sub>E</sub> = 0) (V <sub>CB</sub> = 20 V <sub>dc</sub> , I <sub>E</sub> = 0, T <sub>A</sub> = 100°C)	I <sub>CBO</sub>	–	–	100 10	nA <sub>dc</sub> μA <sub>dc</sub>
<b>ON CHARACTERISTICS</b>					
DC Current Gain (I <sub>C</sub> = 2.0 mA <sub>dc</sub> , V <sub>CE</sub> = 5.0 V <sub>dc</sub> )	h <sub>FE</sub>	200	–	450	–
Collector – Emitter Saturation Voltage (I <sub>C</sub> = 10 mA <sub>dc</sub> , I <sub>B</sub> = 0.5 mA <sub>dc</sub> ) (I <sub>C</sub> = 50 mA <sub>dc</sub> , I <sub>B</sub> = 2.5 mA <sub>dc</sub> )	V <sub>CE(sat)</sub>	– –	– 0.21	0.25 –	V <sub>dc</sub>
Base – Emitter Saturation Voltage (I <sub>C</sub> = 50 mA <sub>dc</sub> , I <sub>B</sub> = 2.5 mA <sub>dc</sub> )	V <sub>BE(sat)</sub>	–	0.85	–	V <sub>dc</sub>
Base – Emitter On Voltage (I <sub>C</sub> = 2.0 mA <sub>dc</sub> , V <sub>CE</sub> = 5.0 V <sub>dc</sub> )	V <sub>BE(on)</sub>	0.6	–	0.75	V <sub>dc</sub>
<b>SMALL – SIGNAL CHARACTERISTICS</b>					
Current – Gain – Bandwidth Product (I <sub>C</sub> = 10 mA <sub>dc</sub> , V <sub>CE</sub> = 5.0 V <sub>dc</sub> , f = 100 MHz)	f <sub>T</sub>	–	300	–	MHz
Output Capacitance (I <sub>E</sub> = 0, V <sub>CB</sub> = 10 V <sub>dc</sub> , f = 1.0 MHz)	C <sub>obo</sub>	–	–	4.0	pF
Input Capacitance (I <sub>E</sub> = 0, V <sub>CB</sub> = 10 V <sub>dc</sub> , f = 1.0 MHz)	C <sub>ibo</sub>	–	9.0	–	pF
Noise Figure (I <sub>C</sub> = 0.2 mA <sub>dc</sub> , V <sub>CE</sub> = 5.0 V <sub>dc</sub> , R <sub>S</sub> = 2.0 kΩ, f = 1.0 kHz, BW = 200 Hz)	NF	–	–	10	dB

## EQUIVALENT SWITCHING TIME TEST CIRCUITS

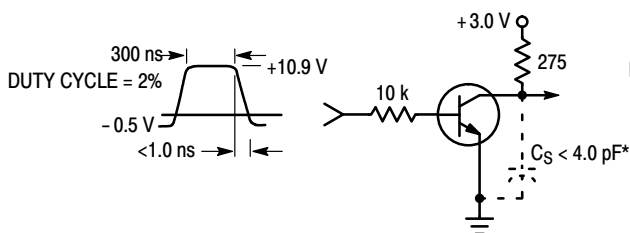


Figure 1. Turn-On Time

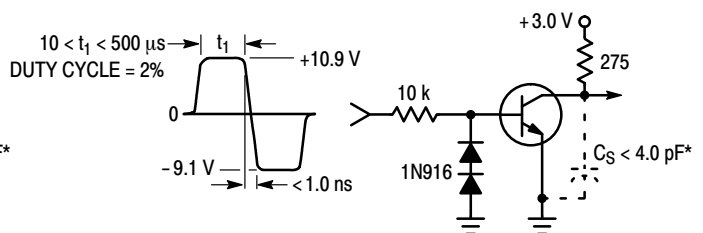


Figure 2. Turn-Off Time

\*Total shunt capacitance of test jig and connectors

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## TYPICAL NOISE CHARACTERISTICS

( $V_{CE} = 5.0 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

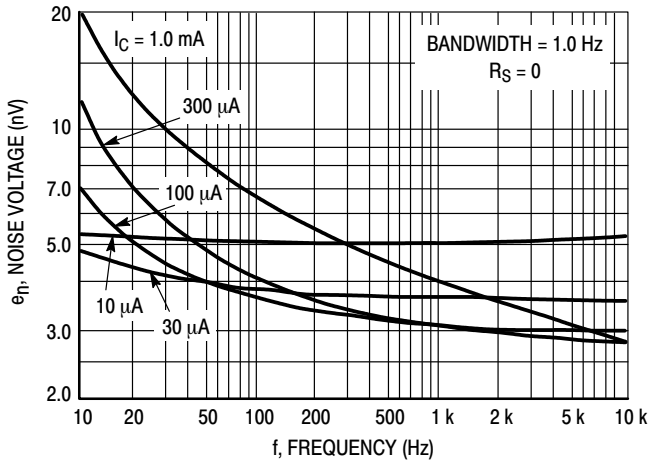


Figure 3. Noise Voltage

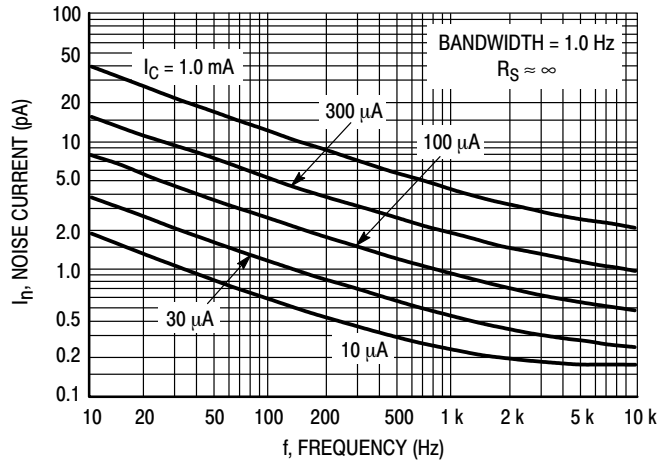


Figure 4. Noise Current

## NOISE FIGURE CONTOURS

( $V_{CE} = 5.0 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

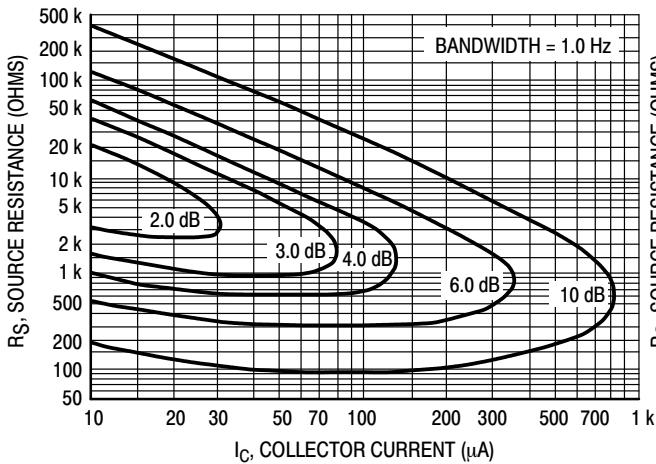


Figure 5. Narrow Band, 100 Hz

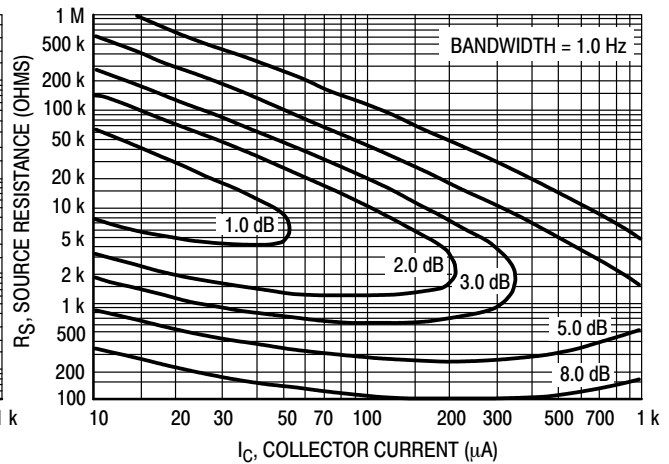


Figure 6. Narrow Band, 1.0 kHz

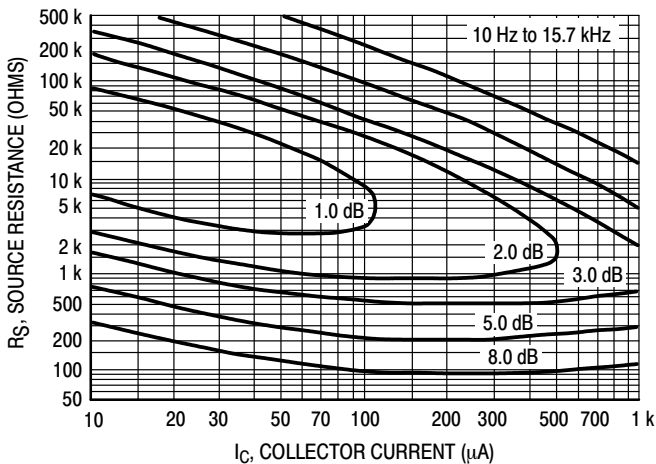


Figure 7. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left( \frac{e_n^2 + 4KTR_S + I_n^2 R_S^2}{4KTR_S} \right)^{1/2}$$

$e_n$  = Noise Voltage of the Transistor referred to the input. (Figure 3)

$I_n$  = Noise Current of the Transistor referred to the input. (Figure 4)

$K$  = Boltzman's Constant ( $1.38 \times 10^{-23} \text{ J}^\circ\text{K}$ )

$T$  = Temperature of the Source Resistance ( $^\circ\text{K}$ )

$R_S$  = Source Resistance (Ohms)

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## TYPICAL STATIC CHARACTERISTICS

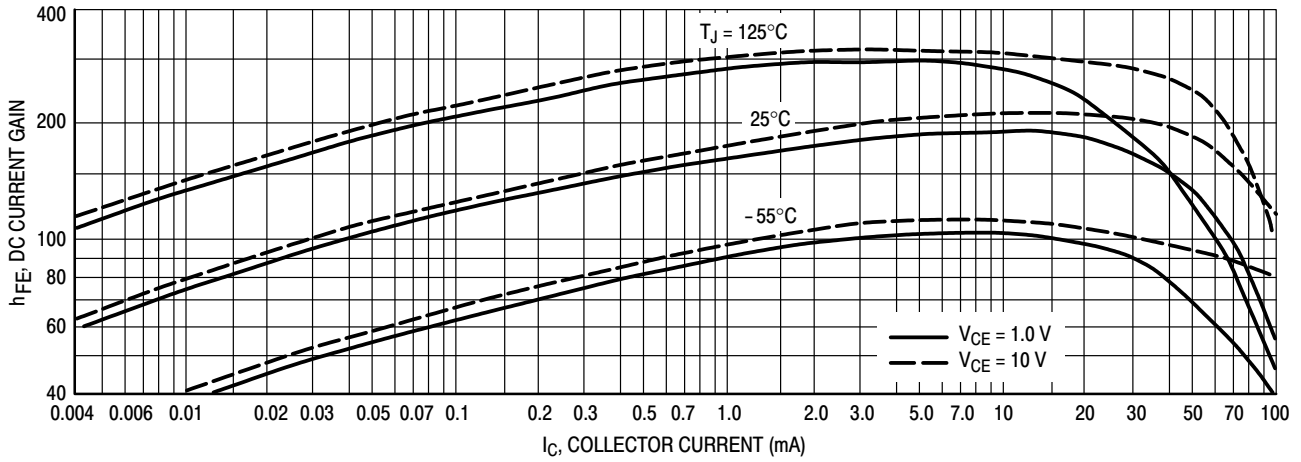


Figure 8. DC Current Gain

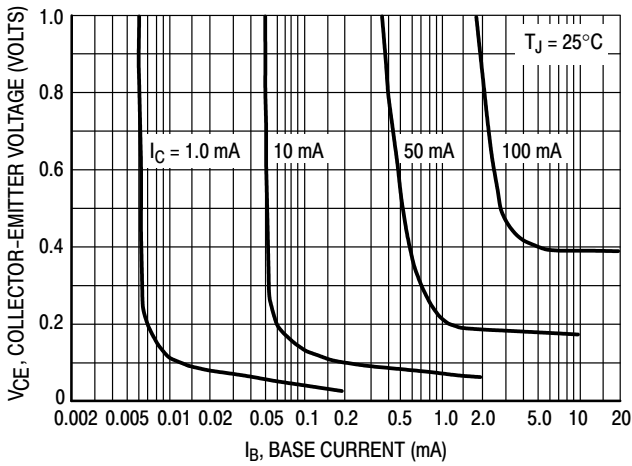


Figure 9. Collector Saturation Region

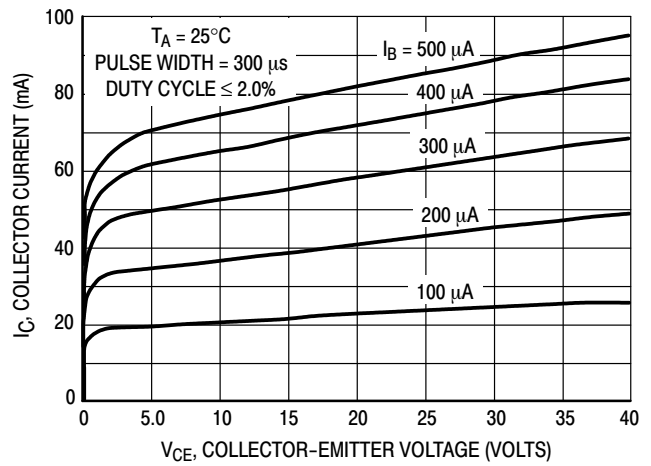


Figure 10. Collector Characteristics

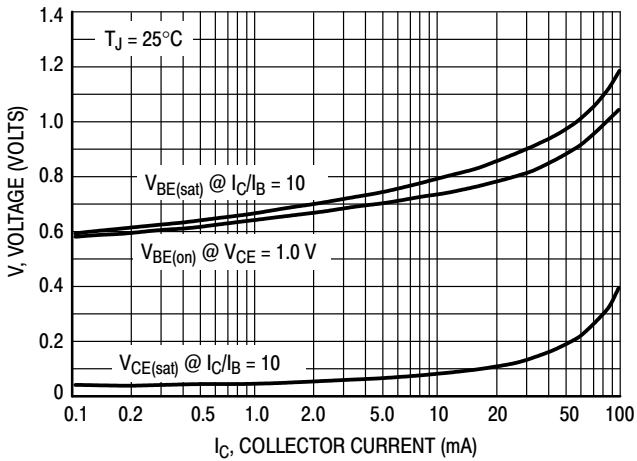


Figure 11. "On" Voltages

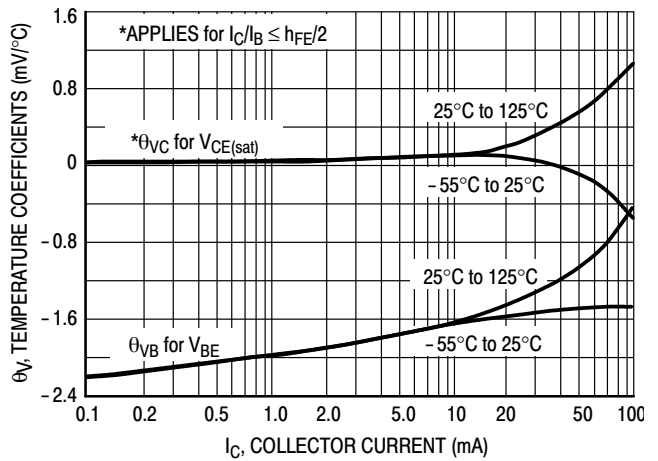


Figure 12. Temperature Coefficients

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## TYPICAL DYNAMIC CHARACTERISTICS

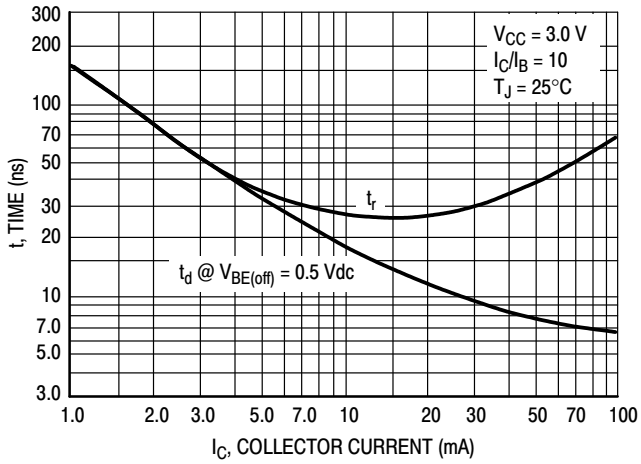


Figure 13. Turn-On Time

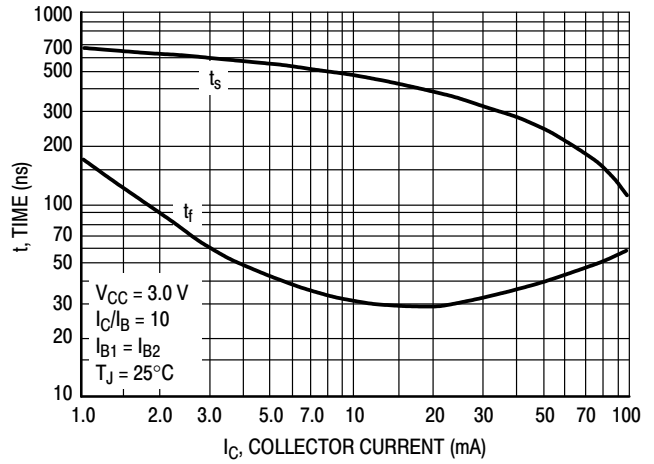


Figure 14. Turn-Off Time

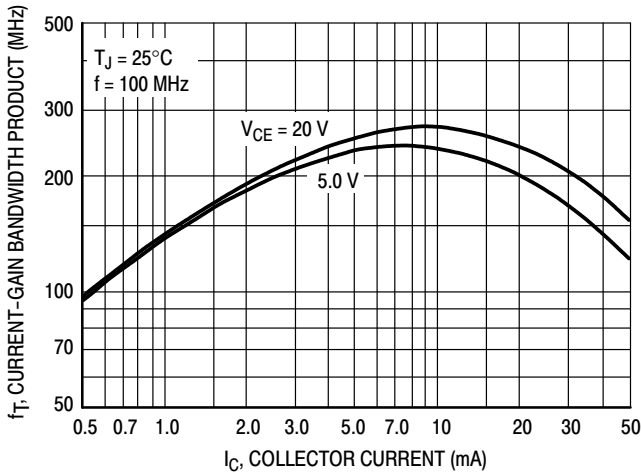


Figure 15. Current-Gain — Bandwidth Product

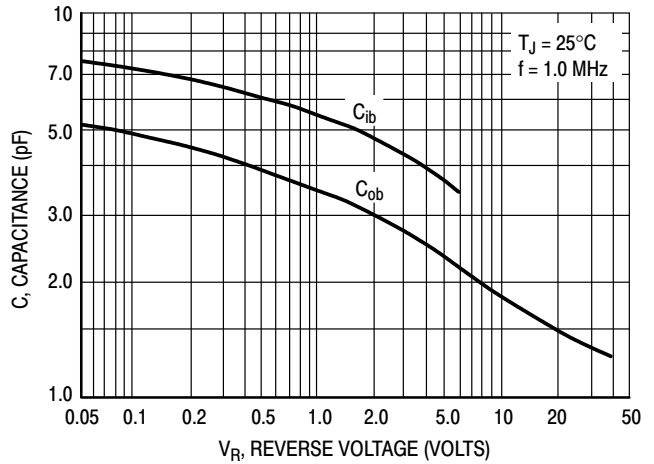


Figure 16. Capacitance

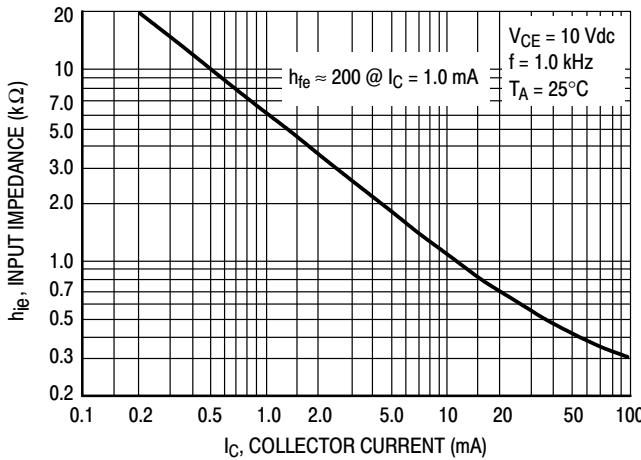


Figure 17. Input Impedance

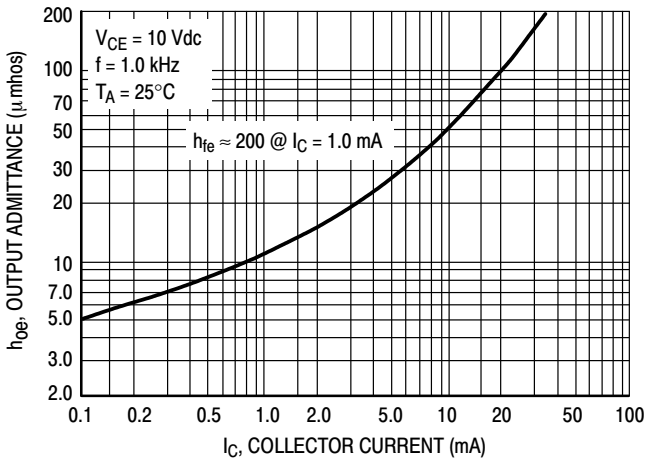


Figure 18. Output Admittance

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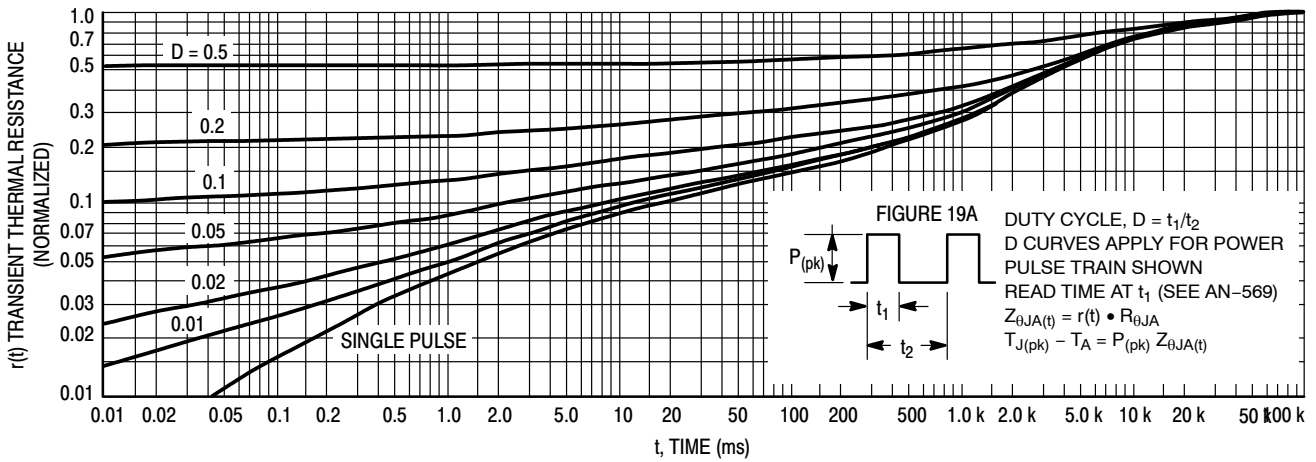


Figure 19. Thermal Response

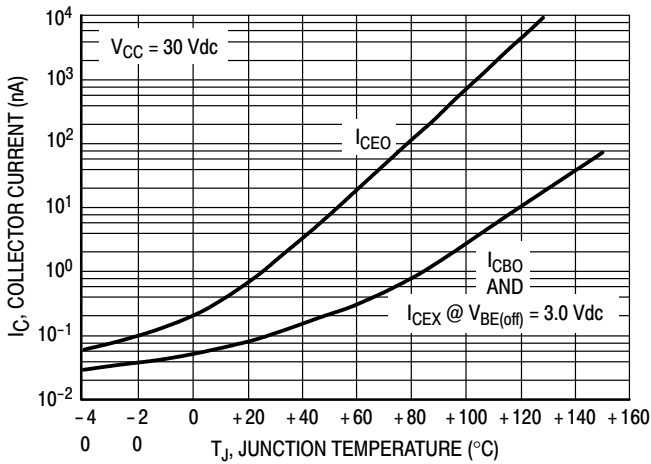


Figure 19A.

### DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 19A. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 19 was calculated for various duty cycles.

To find  $Z_{\theta JA}(t)$ , multiply the value obtained from Figure 19 by the steady state value  $R_{\theta JA}$ .

Example:

The MPS3904 is dissipating 2.0 watts peak under the following conditions:

$$t_1 = 1.0 \text{ ms}, t_2 = 5.0 \text{ ms}. (D = 0.2)$$

Using Figure 19 at a pulse width of 1.0 ms and  $D = 0.2$ , the reading of  $r(t)$  is 0.22.

The peak rise in junction temperature is therefore

$$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88^\circ\text{C}.$$

For more information, see AN-569.

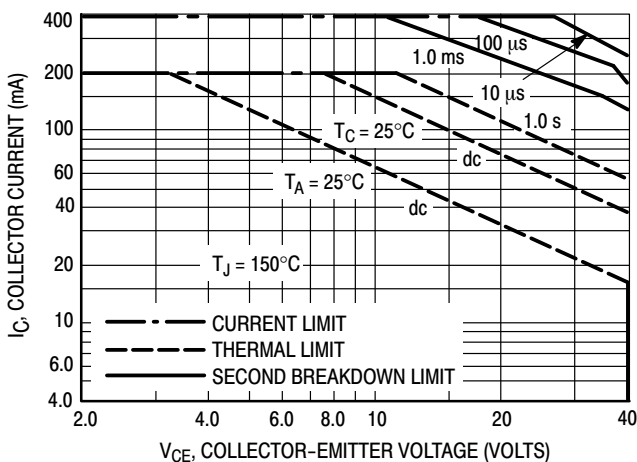


Figure 20.

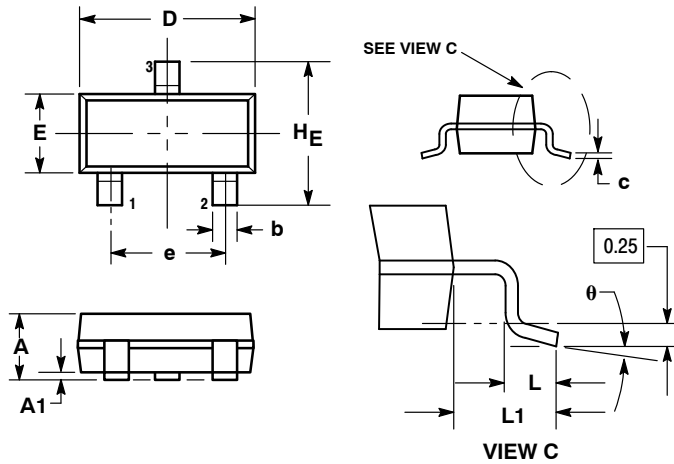
The safe operating area curves indicate  $I_C$ - $V_{CE}$  limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

The data of Figure 20 is based upon  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  or  $T_A$  is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 19. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# BCW72LT1G

## PACKAGE DIMENSIONS

SOT-23 (TO-236)  
CASE 318-08  
ISSUE AN



**NOTES:**

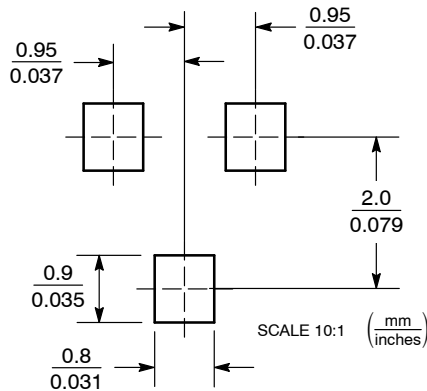
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 318-01 THRU -07 AND -09 OBSOLETE, NEW STANDARD 318-08.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104

**STYLE 6:**

1. BASE
2. EMITTER
3. COLLECTOR

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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