N-Channel Enhancement MOSFET , ESD Protection

GENERAL DESCRIPTION

The ME2320D is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- 20V/6.5A, $R_{DS(ON)}$=21mΩ@V_{GS}=4.5V
- 20V/5.5A, $R_{DS(ON)}$=25 mΩ@V_{GS}=2.5V
- 20V/5A, $R_{DS(ON)}$=33 mΩ@V_{GS}=1.8V
- ESD rating : 4000V HBM
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability

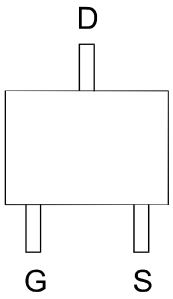
APPLICATIONS

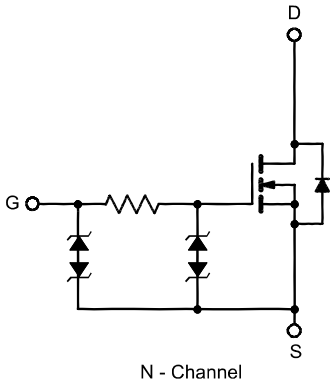
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION

(SOT-23)

Top View





N - Channel

Absolute Maximum Ratings (T_A=25℃ Unless Otherwise Noted)

Parameter		Symbol	Maximum		Unit
Drain-Source Voltage		V_{DSS}	20		V
Gate-Source Voltage		V_{GSS}	±8		V
Continuous Drain Current(tJ=150℃)	T_A=25℃	I_D	6.5		A
	T_A=70℃		5.2		
Pulsed Drain Current		I_{DM}	30		A
Continuous Source Current (Diode Conduction)		I_S	2.5		A
Maximum Power Dissipation	T_A=25℃	P_D	1.4		W
	T_A=70℃		0.9		
Operating Junction Temperature		T_J	-55 to 150		℃
Storage Temperature Range		T_{stg}	-55 to 150		℃
Thermal Resistance-Junction to Ambient*		$R_{\theta JA}$	T≦10 sec	85	℃/W
			Steady State	125	
Thermal Resistance-Junction to Case		$R_{\theta JC}$	75		℃/W

* The device mounted on 1in^2 FR4 board with 2 oz copper

N-Channel Enhancement MOSFET , ESD Protection

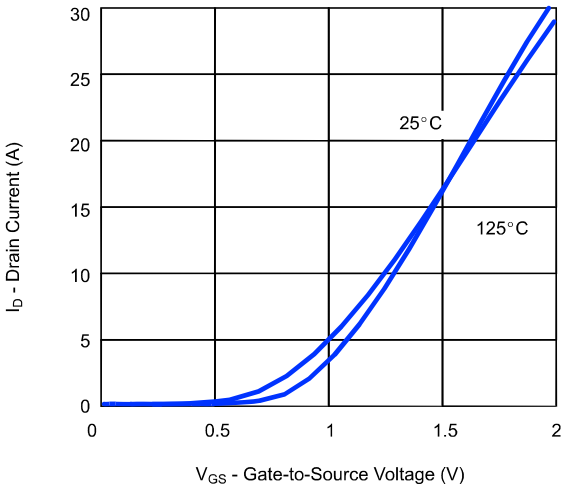
Electrical Characteristics (T_A=25℃ Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	0.4	0.6	1	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±4.5V			±1	μA
		V_{DS}=0V, V_{GS}=±8V			±10	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V			1	μA
		V_{DS}=16V, V_{GS}=0V			1	
		T_J=55℃			5	
$I_{D(ON)}$	On-State Drain Current[a]	V_{DS}=4.5V, V_{GS}= 5V	30			A
$R_{DS(ON)}$	Drain-Source On-Resistance[a]	V_{GS}=4.5V, I_D= 6.5A		17	21	mΩ
		V_{GS}=2.5V, I_D= 5.5A		20	25	
		V_{GS}=1.8V, I_D= 5A		25	33	
V_{SD}	Diode Forward Voltage	I_S=1A, V_{GS}=0V		0.6	1	V
DYNAMIC						
Qg	Total Gate Charge	V_{DS}=10V, V_{GS}=4.5 I_D=6.5A		10	12	nC
Qgs	Gate-Source Charge			0.9		
Qgd	Gate-Drain Charge			3		
Ciss	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1MHz		150	180	pF
Coss	Output Capacitance			95		
Crss	Reverse Transfer Capacitance			25		
$t_{d(on)}$	Turn-On Delay Time	V_{DS}=10V, R_L= 1.5Ω, V_{GS}=5V, R_{GEN}=3Ω		250	300	ns
tr	Turn-On Rise Time			420	500	
$t_{d(off)}$	Turn-Off Delay Time			3950	4200	
tf	Turn-Off Fall Time			3700	3900	

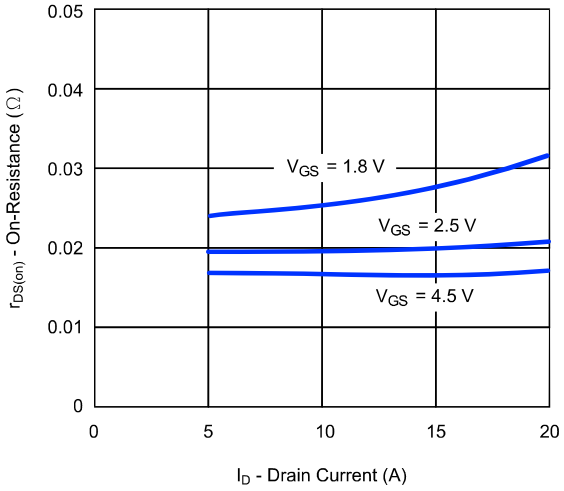
Notes: a. Pulse test; pulse width ≦ 300us, duty cycle≦ 2%

Typical Characteristics (T_J =25℃ Noted)

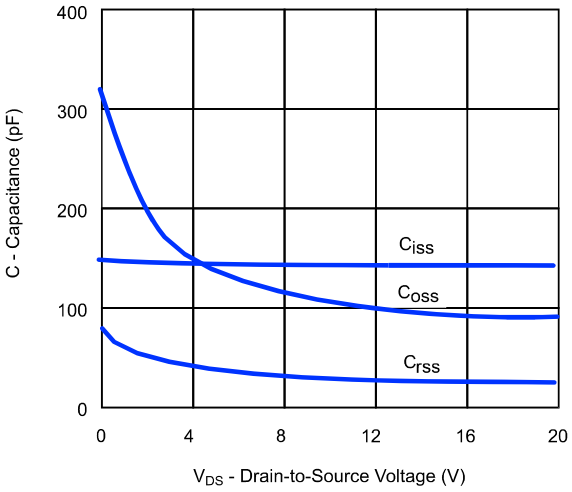
Transfer Characteristics



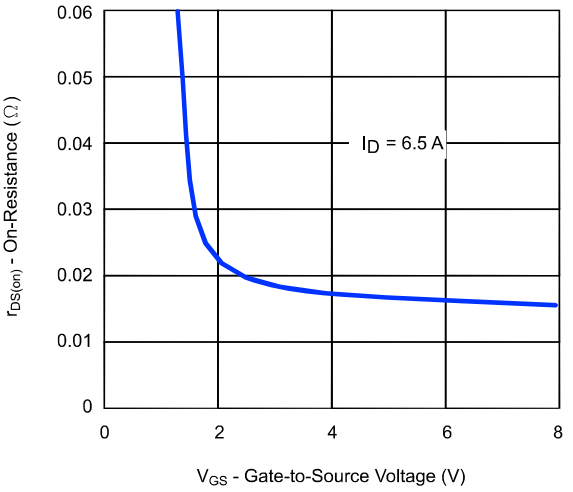
On-Resistance vs. Drain Current



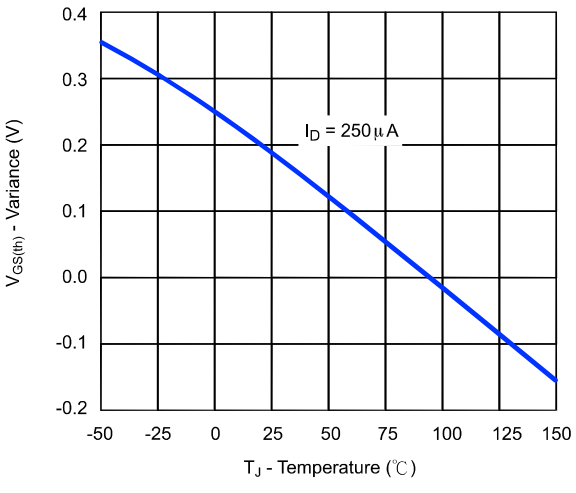
Capacitance



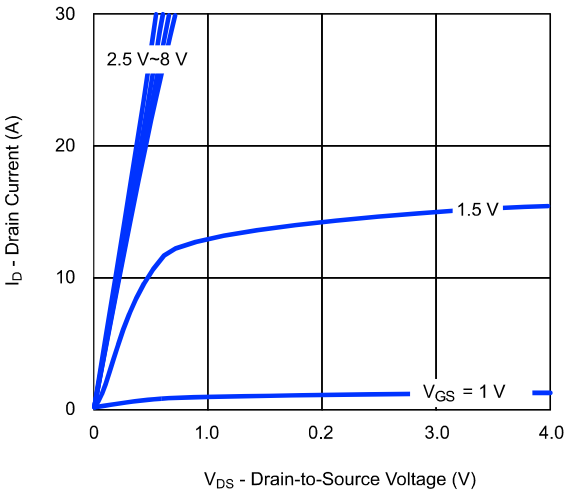
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

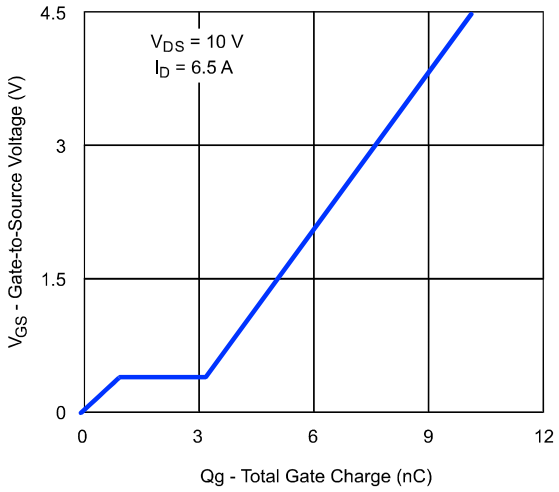


On-Region Characteristics

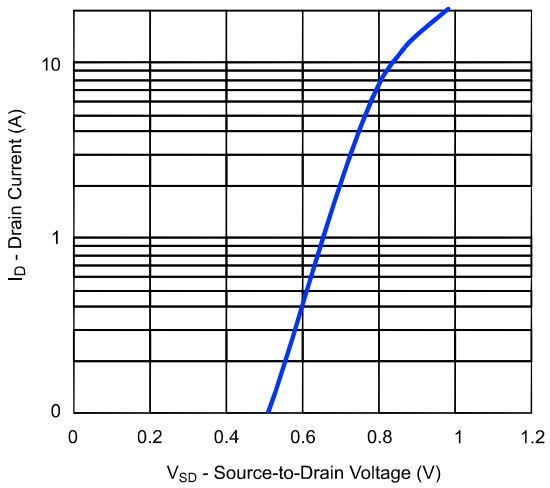


Typical Characteristics (T_J =25℃ Noted)

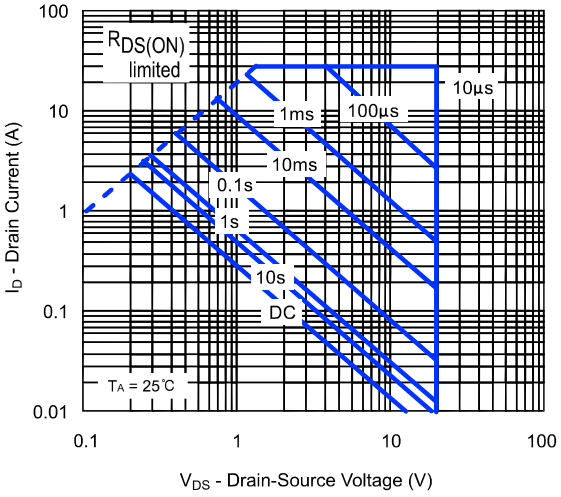
Gate Charge



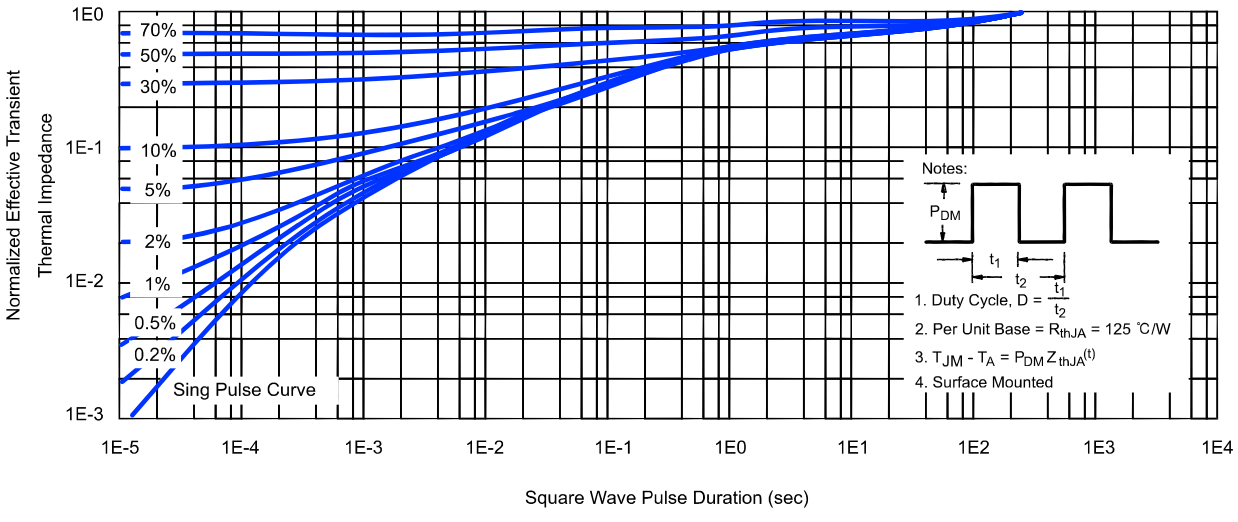
On-Resistance vs. Drain Current



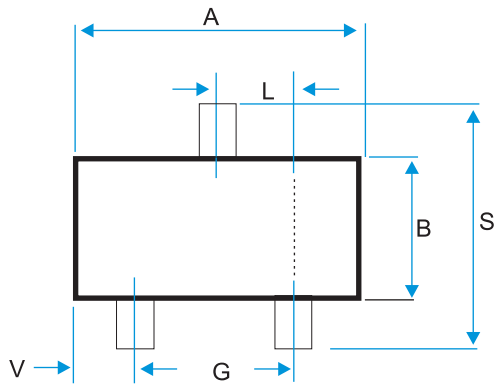
Maximum Forward Biased Safe Operating Area

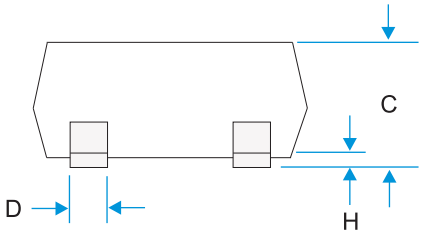


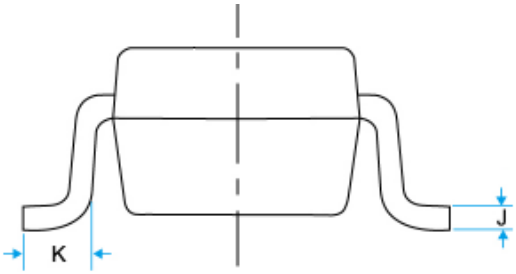
Normalized Thermal Transient Impedance, Junction-to-Ambient



SOT-23 Package Outline







DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60