N-Channel MOSFET

GENERAL DESCRIPTION

The ME2N7002W is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

FEATURES

- $R_{DS(ON)}$= 3.0Ω@V_{GS}=10V, I_D=500mA
- $R_{DS(ON)}$= 4.0Ω@V_{GS}=4.5V, I_D=75mA
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-323 package design

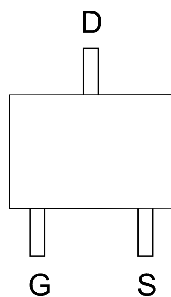
Mechanical data

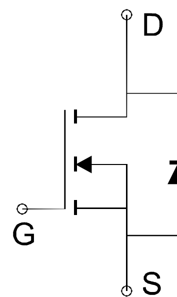
- High density cell design for low $R_{DS(ON)}$
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability.
- The soldering temperature and time shall not exceed 260℃ for more than 10 seconds.

PIN CONFIGURATION

(SOT-323)

Top View





PARAMETER	Symbol	Limits	Units
Drain-Source Voltage	V_{DSS}	60	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current	I_D	115	mA
Pulsed Drain Current (Note 1)	I_{DM}	800	mA
Maximum Power Dissipation T_A =25°C	P_D	200	mW
T_A =75°C		120	
Operating and Storage Temperature Range	T_J ,T_{STG}	-55 ~ +150	°C
Thermal Resistance, Junction-to-Ambient (PCB mounted) (Note 2)	$R_{θJA}$	625	°C/W

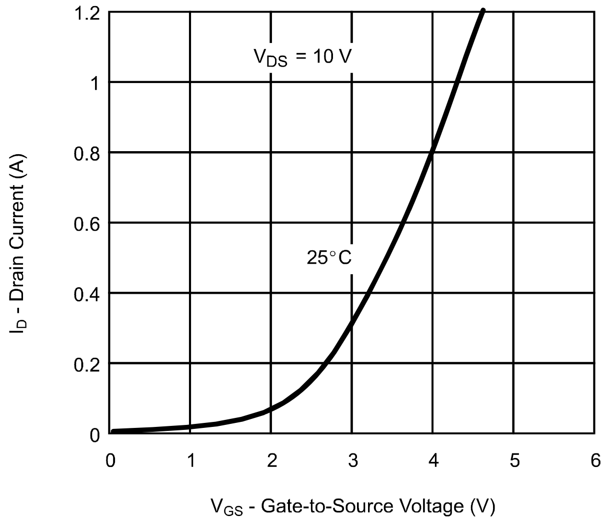
Electrical Characteristics (T_A =25℃ Unless Otherwise Specified)

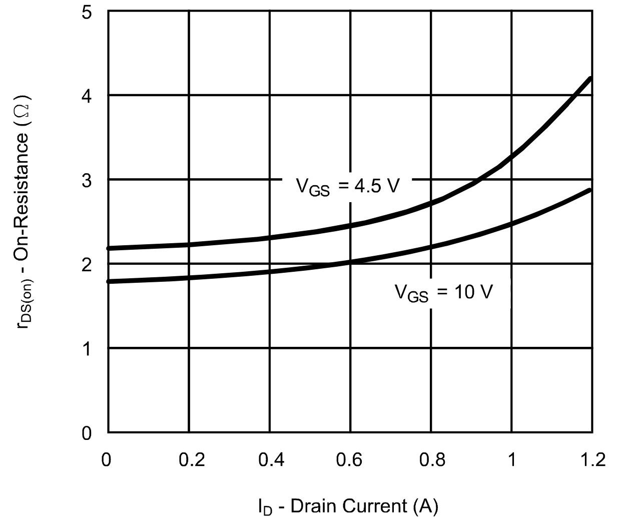
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=10uA	60	-	-	V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	1	-	2.5	V
I_{GSS}	Gate-body Leakage	V_{DS}=0V, V_{GS}= ±20V	-	-	±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	-	-	1	uA
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D=250mA	200	-	-	ms
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V, I_D=500mA	-	1.8	3.0	Ω
		V_{GS}=4.5V, I_D=75mA	-	2.2	4.0	
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input Capacitance	V_{DS}=25V, V_{GS}=0V f=1.0MHz	-	-	50	pF
C_{OSS}	Output Capacitance		-	-	25	
C_{RSS}	Reverse Transfer Capacitance		-	-	5	
Q_G	Total Gate Charge	V_{DS}=15V, I_D=500mA , V_{GS} = 4.5V	-	0.6	0.7	nC
Q_{GS}	Gate-Source Charge		-	0.1	-	
Q_{GD}	Gate-Drain Charge		-	0.08	-	
$TD_{(ON)}$	Turn-On Delay Time	V_{DD}=10V,R_L=20Ω, R_G=10Ω, I_D=500mA, V_{GEN} = 10V	-	9	15	nS
$TD_{(OFF)}$	Turn-Off Delay Time		-	21	26	
Source-Drain Diode						
I_S	Diode Forward Current	-	-	-	300	mA
V_{SD}	Diode Forward Voltage	V_{GS}=0V, I_S =300mA	-	0.93	1.2	V

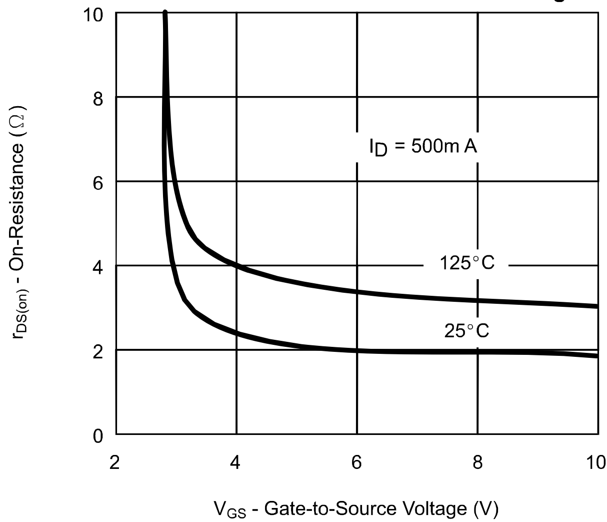
Note :

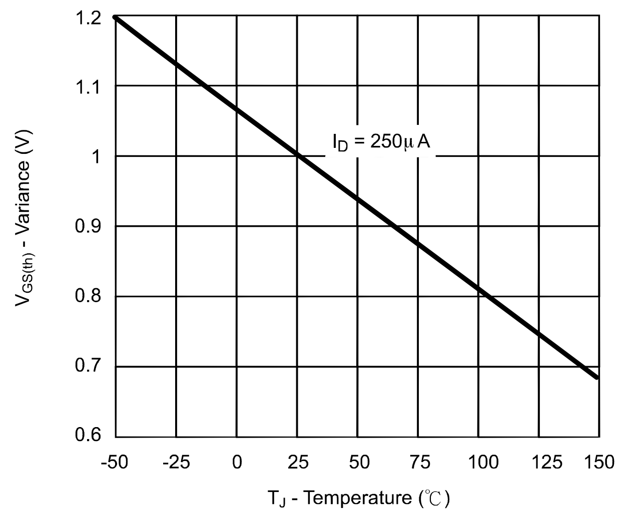
(1) Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

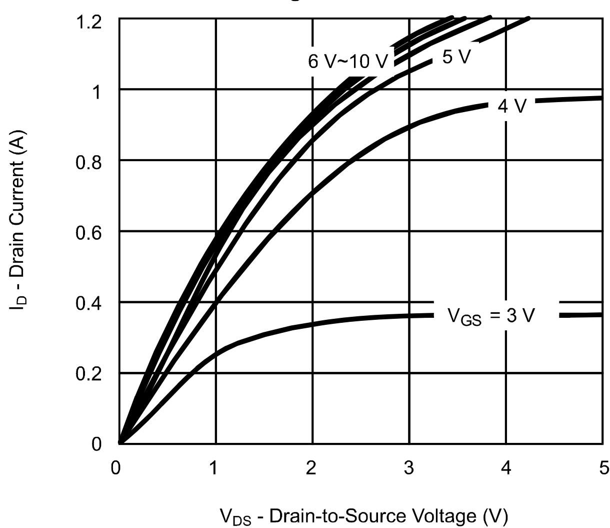
(2) Pulse width limited by safe operating area.

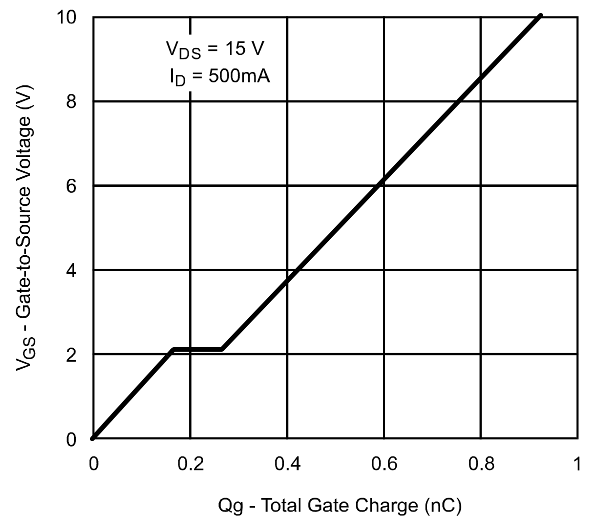

Transfer Characteristics
V_{DS} = 10 V
25°C
I_D - Drain Current (A)
V_{GS} - Gate-to-Source Voltage (V)


On-Resistance vs. Drain Current
V_{GS} = 4.5 V
V_{GS} = 10 V
$r_{DS(on)}$ - On-Resistance (Ω)
I_D - Drain Current (A)

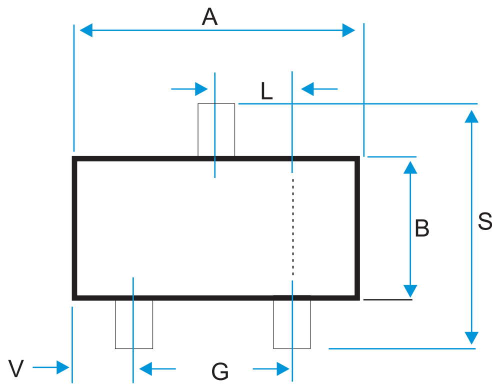

On-Resistance vs. Gate-to-Source Voltage
I_D = 500m A
125°C
25°C
$r_{DS(on)}$ - On-Resistance (Ω)
V_{GS} - Gate-to-Source Voltage (V)

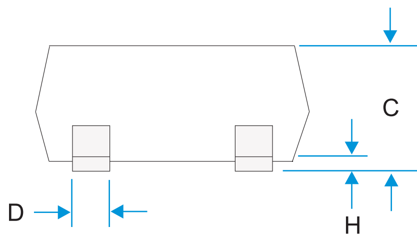

Threshold Voltage
I_D = 250μA
$V_{GS(th)}$ - Variance (V)
T_J - Temperature (℃)

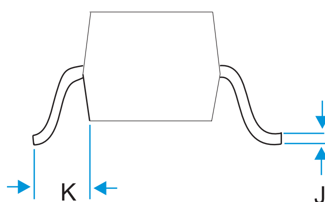

On-Region Characteristics
6 V~10 V
5 V
4 V
V_{GS} = 3 V
I_D - Drain Current (A)
V_{DS} - Drain-to-Source Voltage (V)


Gate Charge
V_{DS} = 15 V
I_D = 500mA
V_{GS} - Gate-to-Source Voltage (V)
Qg - Total Gate Charge (nC)

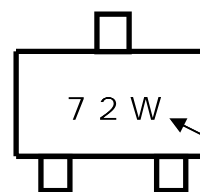
SOT-323 Package







DIM	MILLIMETERS	
	MIN	MAX
A	1.80	2.20
B	1.15	1.35
C	0.90	1.10
D	0.20	0.40
G	1.20	1.40
H	0.00	0.10
J	0.05	0.15
K	0.25	0.4
L	0.25	0.65
S	2.00	2.45
V	0.30	0.40



Body Marking Code :
1. : 72W
2. : K72