Field Effect Transistor Silicon N Channel Junction Type

HB101CTB

For ECM

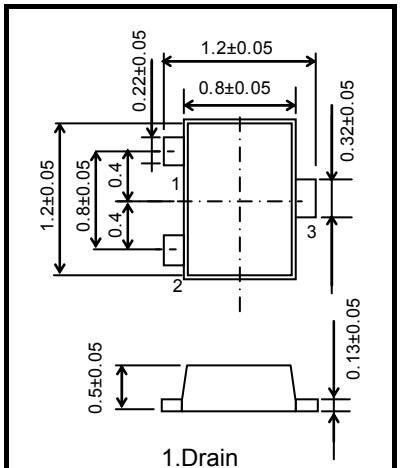
Application for compact ECM

thin package:0.5mm

low capacitance: Ciss = 1.8 pF (typ.) @VDS = 2 V, VGS = 0, f = 1MHzLow noise: V_N = 15 mV (typ.)

@VDD=2 V, RK=1kΩ, Cg=10pF, Gv=80dB, A-Cuve Filter

Unit: mm



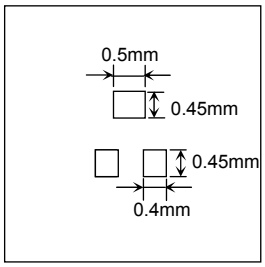
JEDEC	-
JEITA	-

Weight: 1.5mg (typ.)

Absolute Maximum Ratings (Ta=25°C)

Characteristic	Symbol	Rating	Unit
Gate-drain voltage	V_{GDO}	-20	V
Gate current	I_G	10	mA
Drain power dissipation	P_D (Note 1)	150	mW
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C

Note 1: Mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t)

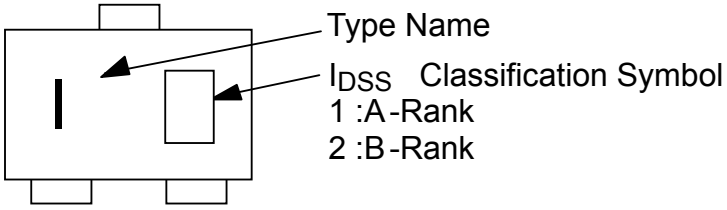


I_{DSS} CLASSIFICATION

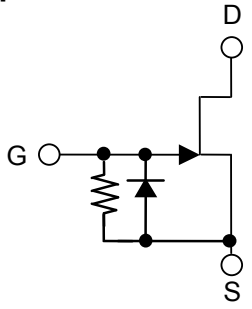
A-Rank 140 to 240 μA

B-Rank 210 to 350 μA

Marking



Equivalent Circuit

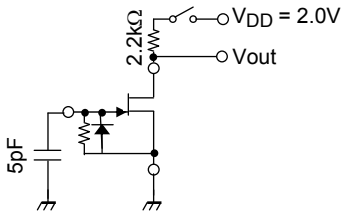


Electrical Characteristics (Ta=25°C)

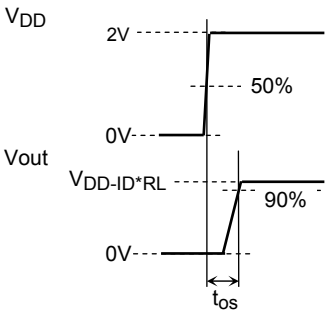
Characteristic	Symbol	Test Condition		Min	Typ.	Max	Unit
Drain current	I_{DSS}	V_{DS} = 2 V, V_{GS} = 0	A	140	—	240	μA
			B	210	—	350	
Drain current	I_D	V_{DD} = 2 V, RL= 2.2kΩ,Cg = 5pF	A	125	—	260	μA
			B	190	—	370	
Gate-source cut-off voltage	$V_{GS(OFF)}$	V_{DS} = 2 V, I_D = 1μA		-0.1	—	-1.0	V
Forward transfer admittance	$\|Y_{fs}\|$	V_{DS} = 2 V, V_{GS} = 0V		0.65	0.9	—	mS
Gate-drain breakdown voltage	$V_{(BR)GDO}$	IG = -100 μA		-20	—	—	V
Input capacitance	C_{iss}	V_{DS} = 2 V, V_{GS} = 0, f = 1 MHz		—	1.8	—	pF
Voltage gain	Gv	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF, f = 1kHz,vin=100mV	A	-2.7	-1.3	—	dB
			B	-1.8	-0.6	—	
Delta voltage gain	DGv(f)	V_{DD} = 2V, RL= 2.2kΩ,Cg = 5pF,f = 1kHz to 100Hz,vin=100mV		—	0	-1.0	dB
Delta voltage gain	DGv(V)	V_{DD} = 2 V to 1.5 V, RL = 2.2 kΩ, Cg = 5pF,f = 1kHz, vin=100mV	A	—	-0.7	-1.4	dB
			B	—	-1.4	-3.0	
Noise voltage	VN	V_{DD} = 2 V, RL = 1 kΩ, Cg = 10 pF, Gv = 80 dB, A-Curve Filter		—	15	30	mV
Total harmonic distortion	THD	V_{DD} = 2 V, RL = 2.2kΩ, Cg = 5 pF, f = 1kHz, vin = 50mV	A	—	1.1	—	%
			B	—	0.6	—	
Time output stability	tos	V_{DD} = 2 V, RL = 2.2 kΩ, Cg = 5 pF		—	20	50	ms

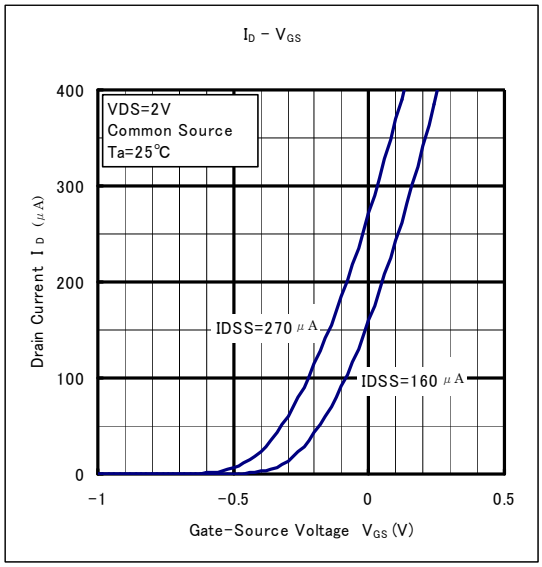
Time Output Stability Test Method

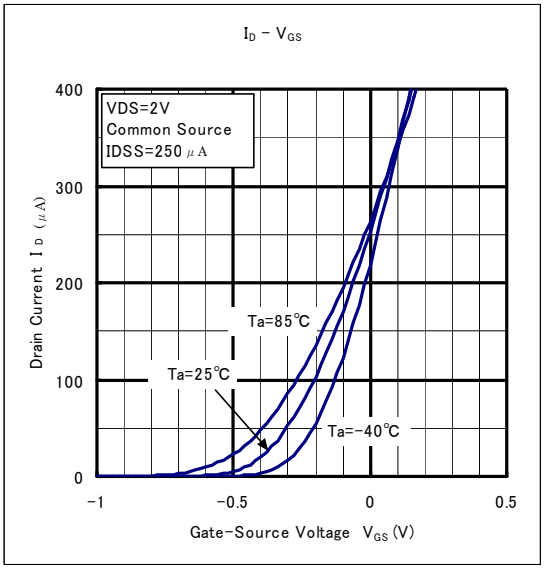
a) TEST CIRCUIT

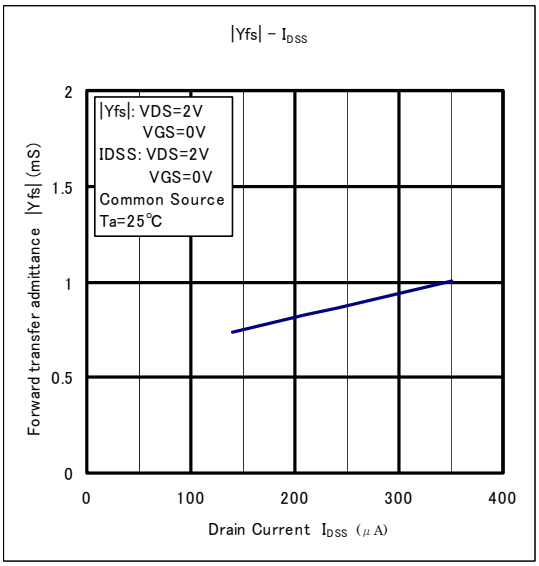


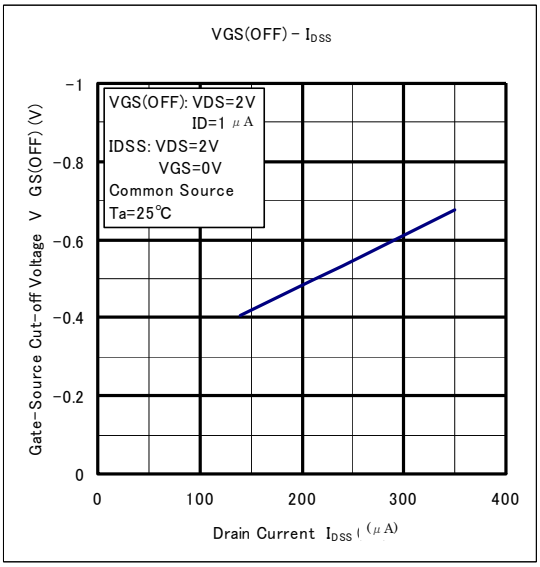
b) TEST SIGNAL

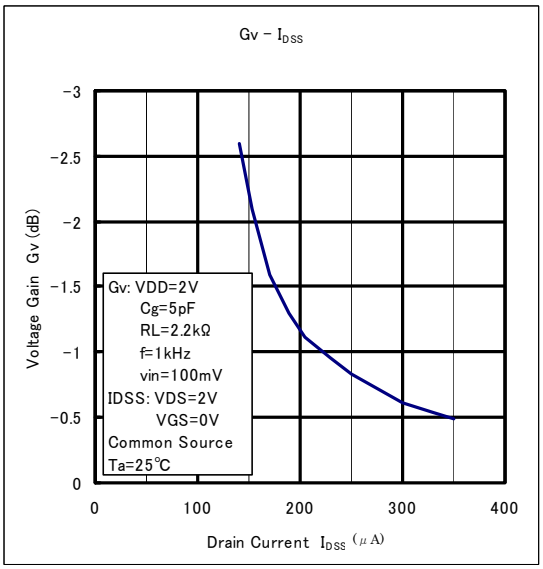


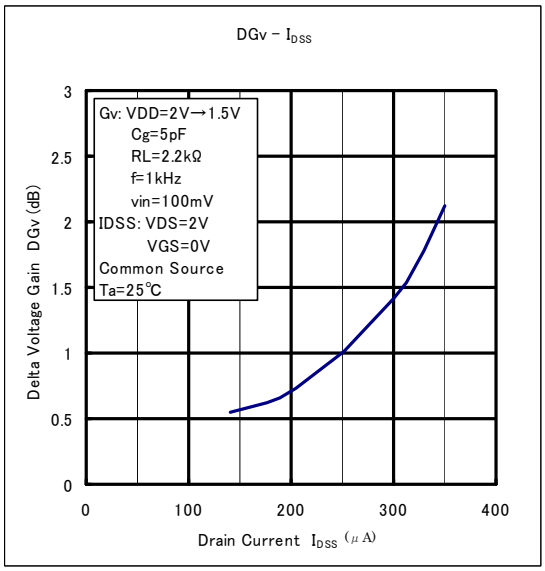

$I_D - V_{GS}$
VDS=2V
Common Source
Ta=25℃
IDSS=270 μA
IDSS=160 μA
Drain Current I_D (μA)
Gate-Source Voltage V_{GS} (V)
400
300
200
100
0
−1
−0.5
0
0.5

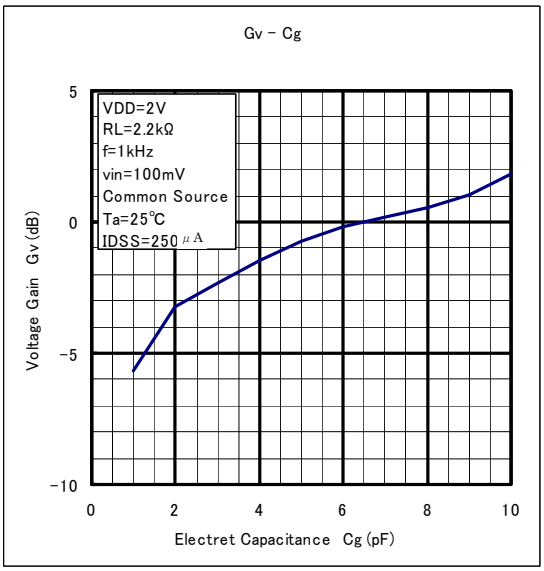

$I_D - V_{GS}$
VDS=2V
Common Source
IDSS=250 μA
Ta=85℃
Ta=25℃
Ta=−40℃
Drain Current I_D (μA)
Gate-Source Voltage V_{GS} (V)
400
300
200
100
0
−1
−0.5
0
0.5

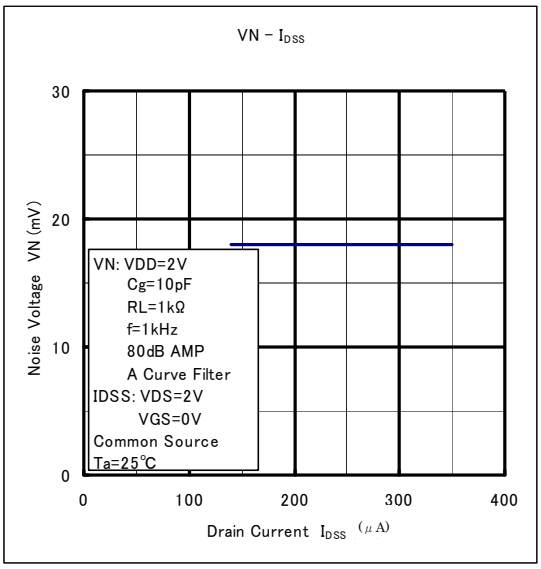

$|Yfs| - I_{DSS}$
|Yfs|: VDS=2V
VGS=0V
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Forward transfer admittance |Yfs| (mS)
Drain Current I_{DSS} (μA)
2
1.5
1
0.5
0
0
100
200
300
400

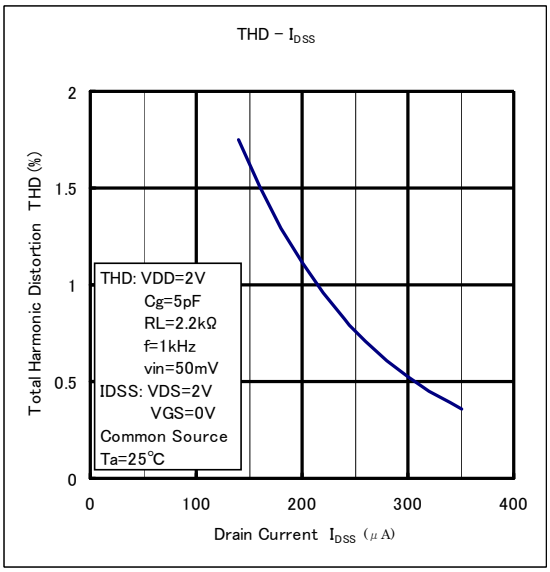

VGS(OFF) - I_{DSS}
VGS(OFF): VDS=2V
ID=1 μA
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Gate-Source Cut-off Voltage V GS(OFF) (V)
Drain Current I_{DSS} (μA)
−1
−0.8
−0.6
−0.4
−0.2
0
0
100
200
300
400

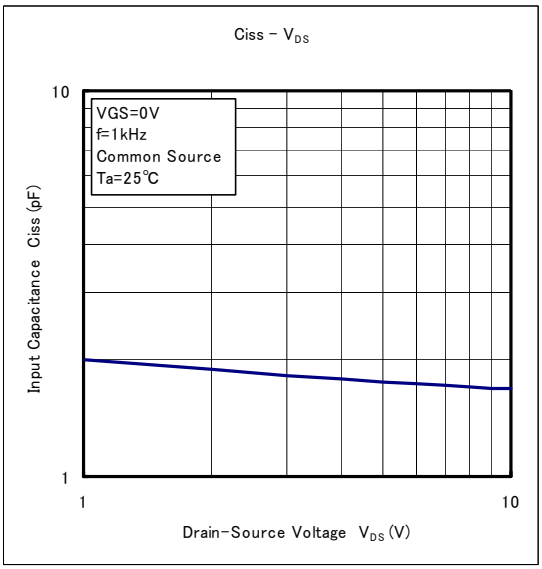

$Gv - I_{DSS}$
Gv: VDD=2V
Cg=5pF
RL=2.2kΩ
f=1kHz
vin=100mV
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Voltage Gain Gv (dB)
Drain Current I_{DSS} (μA)
−3
−2.5
−2
−1.5
−1
−0.5
0
0
100
200
300
400


DGv - I_{DSS}
Gv: VDD=2V→1.5V
Cg=5pF
RL=2.2kΩ
f=1kHz
vin=100mV
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Delta Voltage Gain DGv (dB)
Drain Current I_{DSS} (μA)
3
2.5
2
1.5
1
0.5
0
0
100
200
300
400


Gv – Cg
VDD=2V
RL=2.2kΩ
f=1kHz
vin=100mV
Common Source
Ta=25℃
IDSS=250μA
Voltage Gain Gv (dB)
Electret Capacitance Cg (pF)
5
0
-5
-10
0
2
4
6
8
10


VN – IDSS
VN: VDD=2V
Cg=10pF
RL=1kΩ
f=1kHz
80dB AMP
A Curve Filter
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Noise Voltage VN (mV)
Drain Current IDSS (μA)
30
20
10
0
0
100
200
300
400


THD – IDSS
THD: VDD=2V
Cg=5pF
RL=2.2kΩ
f=1kHz
vin=50mV
IDSS: VDS=2V
VGS=0V
Common Source
Ta=25℃
Total Harmonic Distortion THD (%)
Drain Current IDSS (μA)
2
1.5
1
0.5
0
0
100
200
300
400


Ciss – VDS
VGS=0V
f=1kHz
Common Source
Ta=25℃
Input Capacitance Ciss (pF)
Drain-Source Voltage VDS (V)
10
1
1
10