Field-Effect Transistor Silicon P-Channel MOS Type (U-MOSVI)

○Power Management Switch Applications

Unit: mm

- Low ON-resistance: $R_{DS(ON)}$ = 71 mΩ (max) (@V_{GS} = -10 V)
  $R_{DS(ON)}$ = 105 mΩ (max) (@V_{GS} = -4.5 V)
  $R_{DS(ON)}$ = 136 mΩ (max) (@V_{GS} = -4.0 V)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-Source voltage		V_{DSS}	-30	V
Gate-Source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D (Note 1)	-4	A
	Pulse	I_{DP} (Note 1,2)	-16	
Power dissipation	P_D (Note 3)		1	W
	t < 10s		2	
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

1: Gate
2: Source
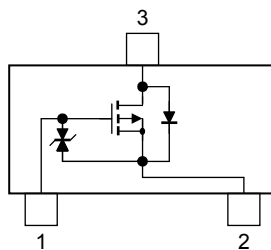3: Drain

SOT-23F
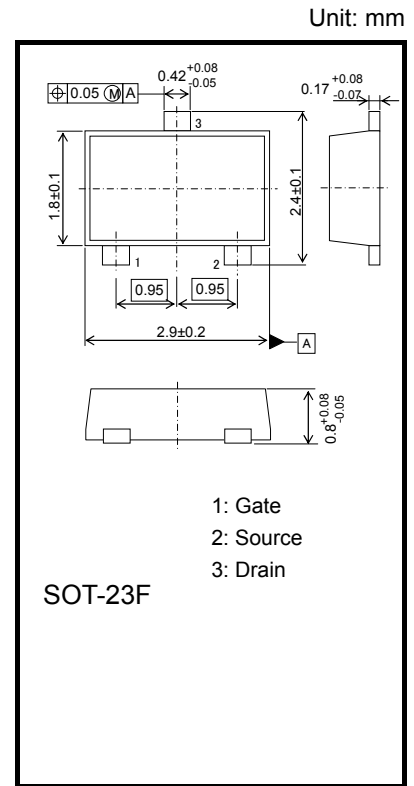
Weight: 11 mg (typ.)

Marking

KFL
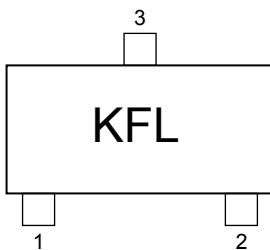
Equivalent Circuit (Top View)

Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Conditions		Min	Typ.	Max	Unit
Drain-Source breakdown voltage		$V_{(BR)DSS}$	I_D = -10 mA, V_{GS} = 0 V		-30	—	—	V
		$V_{(BR)DSX}$	I_D = -10 mA, V_{GS} = 10 V	(Note 5)	-21	—	—	V
Drain cut-off current		I_{DSS}	V_{DS} = -30 V, V_{GS} = 0 V		—	—	-1	μA
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V		—	—	±10	μA
Gate threshold voltage		V_{th}	V_{DS} = -10 V, I_D = -100 μA		-0.8	—	-2.0	V
Forward transfer admittance		$|Y_{fs}|$	V_{DS} = -10 V, I_D = -1.0 A	(Note 4)	2.3	4.6	—	S
Drain–source ON-resistance		$R_{DS(ON)}$	I_D = -3.0 A, V_{GS} = -10 V	(Note 4)	—	54	71	mΩ
			I_D = -2.0 A, V_{GS} = -4.5 V	(Note 4)	—	80	105	
			I_D = -1.0 A, V_{GS} = -4.0 V	(Note 4)	—	89	136	
Input capacitance		C_{iss}	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		—	280	—	pF
Output capacitance		C_{oss}			—	55	—	
Reverse transfer capacitance		C_{rss}			—	40	—	
Switching time	Turn-on time	t_{on}	V_{DD} = -15 V, I_D = -1.0 A, V_{GS} = 0 to -4.5 V, R_G = 10 Ω		—	13	—	ns
	Turn-off time	t_{off}			—	22	—	
Total Gate Charge		Q_g	V_{DD} = -15 V, I_D = -4.0 A, V_{GS} = -10 V		—	5.9	—	nC
Gate-Source Charge		Q_{gs1}			—	0.8	—	
Gate-Drain Charge		Q_{gd}			—	1.2	—	
Drain-Source forward voltage		V_{DSF}	I_D = 4.0 A, V_{GS} = 0 V	(Note 4)	—	0.9	1.2	V

Note4: Pulse test

Note5: If a forward bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

(a) Test Circuit
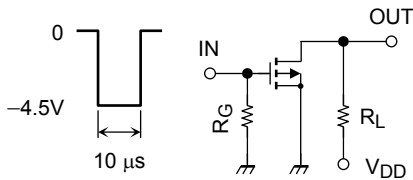
V_{DD} = -15 V
R_G = 10 Ω
Duty. ≤ 1%
V_{IN}: t_r, t_f < 5 ns
Common Source
Ta = 25°C

(b) V_{IN}

(c) V_{OUT}

$I_D - V_{DS}$

Drain current I_D (A)

Drain–source voltage V_{DS} (V)

Common Source
Ta = 25 °C
Pulse test

-10 V   -4.5 V

V_{GS} = -4.0 V

$I_D - V_{GS}$

Drain current I_D (A)

Gate–source voltage V_{GS} (V)

Common Source
V_{DS} = -10 V
Pulse test

Ta = 100 °C
−25 °C
25 °C

$R_{DS (ON)} - V_{GS}$

Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)

Gate–source voltage V_{GS} (V)

I_D = -1.0 A
Common Source
Pulse test

Ta = 100 °C
25 °C
− 25 °C

$R_{DS (ON)} - V_{GS}$

Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)

Gate–source voltage V_{GS} (V)

I_D = -2.0 A
Common Source
Pulse test

Ta = 100 °C
25 °C
− 25 °C

$R_{DS (ON)} - I_D$

Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)

Drain current I_D (A)

Common Source
Ta = 25 °C
Pulse test

-4.0 V
-4.5 V
V_{GS} = -10 V

$R_{DS (ON)} - Ta$

Drain–source ON-resistance $R_{DS (ON)}$ (mΩ)

Ambient temperature Ta (°C)

Common Source
Pulse test

I_D = -1.0 A / V_{GS} = -4.0 V
-2.0 A / -4.5 V
-3.0 A / -10 V

$V_{th} - T_a$

Gate threshold voltage V_{th} (V)

Common Source
V_{DS} = -10 V
I_D = -100 μA

Ambient temperature T_a (°C)

$|Y_{fs}| - I_D$

Forward transfer admittance $|Y_{fs}|$ (S)

Common Source
V_{DS} = -10 V
T_a = 25 °C
Pulse test

Drain current I_D (A)

$C - V_{DS}$

Capacitance C (pF)

C_{iss}
C_{oss}
C_{rss}

Common Source
T_a = 25 °C
f = 1 MHz
V_{GS} = 0 V

Drain–source voltage V_{DS} (V)

Dynamic Input Characteristic

Gate–source voltage V_{GS} (V)

V_{DD} = -15 V
V_{DD} = -24 V

Common Source
I_D = -4.0 A
T_a = 25 °C

Total Gate Charge Q_g (nC)

$t - I_D$

Switching time t (ns)

Common Source
V_{DD} = -15 V
V_{GS} = 0 to -4.5 V
T_a = 25 °C
R_G = 10Ω

t_{off}
t_f
t_{on}
t_r

Drain current I_D (A)

$I_{DR} - V_{DS}$

Drain reverse current I_{DR} (A)

Common Source
V_{GS} = 0 V
Pulse test

100 °C
25 °C
-25 °C

Drain–source voltage V_{DS} (V)

rth − tw

Single pulse
a. Mounted on FR4 board
   (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)
b. Mounted on FR4 board
   (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 0.72 mm² ×3)

$P_D - T_a$

a: Mounted on FR4 board
   (25.4mm × 25.4mm × 1.6mm, Cu Pad: 645 mm²)
b: Mounted on FR4 board
   (25.4mm × 25.4mm × 1.6mm, Cu Pad: 0.72 mm² ×3)